

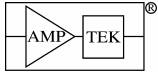
## User's Guide and Operating Instructions

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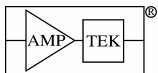
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1	DP4 Design and Operation .....	3
1.1	Major Function Blocks.....	3
1.2	DP4 Input .....	4
1.3	Pulse Shaping and Selection .....	5
1.4	DP4 Interface .....	10
2	DP4 Specifications .....	11
2.1	Connections .....	11
	Controls and Adjustments .....	15
3	Quick Start Instructions .....	18
3.1	Set-Up Instructions .....	19
3.2	Configuring the DP4.....	21
3.3	Taking data .....	21
4	Control and Display Demonstration Software .....	23
5	Programmer's Guide .....	26
5.1	RS232 Serial Interface.....	26
5.2	USB Interface.....	26
6	Use of the DP4 with Amptek's XR100 Detectors .....	35
6.1	Users with a Standard XR100 and PX2.....	35
6.2	Users with a Standard XR100 without a PX2 .....	38
6.3	Users with a DP4, PC4-3, and PA-210 Peamplifier.....	39
6.4	Analog Prefilter Circuit Description .....	41
6.5	Procedures for Common Changes .....	43
7	Dead Time in the Amptek DP4.....	46
7.1	Fast Channel.....	46
7.2	Slow Channel .....	47



7.3	Acquisition Time.....	48
7.4	Timing Summary.....	49
8	Trouble-Shooting Guide .....	49
9	Index.....	49



## 1 DP4 DESIGN AND OPERATION

### 1.1 MAJOR FUNCTION BLOCKS

The DP4 is a component in the complete signal processing chain of a nuclear instrumentation system, as shown in Figure 1. The input to the DP4 is the preamplifier output. The DP4 digitizes the preamplifier output, applies real-time digital processing to the signal, detects the peak amplitude (digitally), and bins this value in its histogramming memory, generating an energy spectrum. The spectrum is then transmitted over the DP4's serial interface to the user's computer.

The Amptek DP4 has 6 main function blocks to implement these functions: (1) an analog prefilter, (2) an ADC, (3) a digital pulse shaper, (4) pulse selection logic, (5) histogram logic, and (6) interfacing hardware (which includes a microcontroller) and software. These six functions will be discussed below. Clearly, the DP4 must be used with other components, including (at a minimum) a detector and preamplifier, a computer with a serial interface and software to communicate, and a power supply.

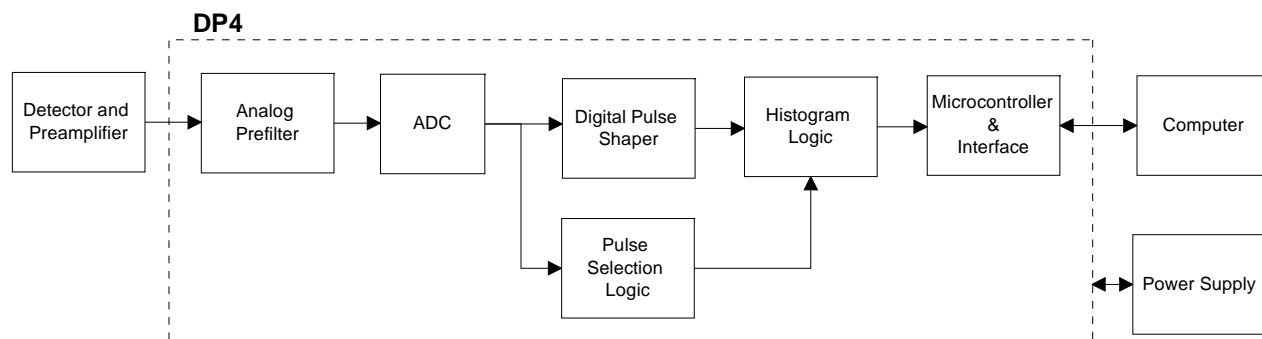


Figure 1. Block diagram of the DP4 in a complete system.

It is important to recognize that the DP4 is designed for OEM use as part of a complete instrument. It can also be tailored for laboratory use, but it is not intended as a stand-alone module for general purpose use. Amptek's PX4 is a general purpose laboratory module which includes the functionality of the DP4 and much more, such as power supplies. Amptek strongly recommends the PX4 for non-OEM users.

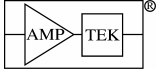
The DP4 interface and control hardware are designed with considerable flexibility so the OEM user can tailor it to a specific application. Amptek supplies software with the DP4 that includes two fully functional demonstration programs. One program runs on the embedded microcontroller and interfaces between the pulse shaping/histogram functions and a PC. The other program runs on a PC and interfaces between the DP4 and the user. Both of these are intended as demonstration programs, which the user will tailor. The DP4 also includes an FPGA. The FPGA logic, the "FPGA Configuration Bitstream", is copyrighted by Amptek, Inc. and may not be copied, modified, or used without the express, written approval of Amptek, Inc.

**Analog Prefilter:** The input to the DP4 is the output of a charge sensitive preamplifier. The analog prefilter circuit prepares this signal for accurate digitization. The main functions of this circuit are (1) applying appropriate gain, offset, and inversion (if necessary) to utilize the dynamic range of the ADC, and (2) carrying out some filtering and pulse shaping functions to optimize the digitization.

**ADC:** The ADC digitizes the output of the analog prefilter at a 20 MHz rate. This stream of digitized values is sent, in real time, into the digital pulse shaper.

**Digital Pulse Shaper:** The ADC output is processed continuously using a pipeline architecture to generate a real time shaped pulse. This carries out pulse shaping as in any other shaping amplifier. The shaped pulse is a purely digital entity. Its output can be routed to a DAC, for diagnostic purposes, but this is not necessary. The peak value of the digital shaped pulse is determined by a peak detect circuit in the pulse shaper. The peak value for each pulse, a single digital quantity, is the primary output of the pulse shaper.

**Pulse Selection Logic:** The pulse selection logic rejects pulses for which an accurate measurement cannot be made. It includes pile-up rejection and risetime discrimination. These are discussed in more detail below.



**Histogram Memory:** The histogram memory operates as in a traditional MCA. When a pulse occurs with a particular peak value, a counter in a corresponding memory location is incremented. The result is a histogram, an array containing, in each cell, the number of events with the corresponding peak value. This is the energy spectrum and is the primary output of the DP4. The DP4 uses 3 bytes per channel, which allows up to 16.7M counts per channel.

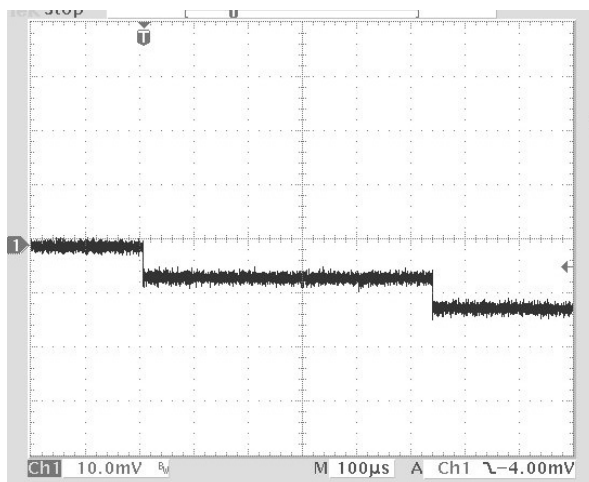
**Interface:** The DP4 includes hardware and software to interface between these various functions and the user's computer. A primary function of the interface is to transmit the spectrum to the user. The interface also controls data acquisition, by starting and stopping the processing and by clearing the histogram memory. It also controls certain aspects of the analog and digital shaping, for example setting the analog gain or the pulse peaking time.

The interface includes a microcontroller and serial interface hardware. Both RS232 and USB interfaces are currently implemented and described in this manual. The interface also contains an I<sup>2</sup>C interface and several unallocated microcontroller pins that are available to the user. The interface includes two distinct software packages, embedded software which runs on the microcontroller on the DP4 and acquisition and control software that runs on the attached personal computer. The DP4 is shipped with a demonstration version of the acquisition and control software package ( Visual Basic 5 source code is provided.) Source code for the embedded software (8051 assembly language) is also available – contact Amptek for more information.

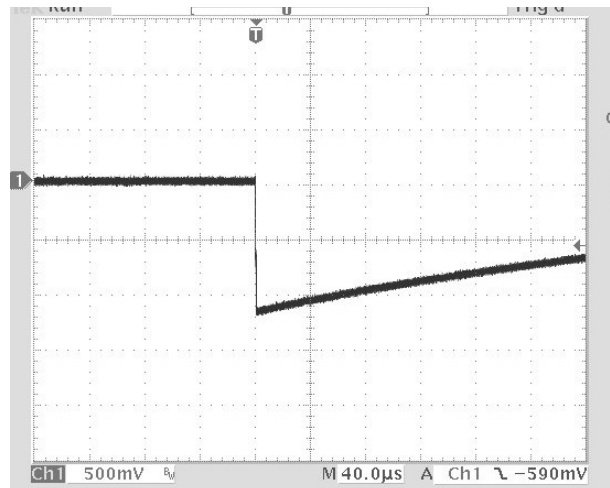
## 1.2 DP4 INPUT

The DP4 was designed to process signals coming directly from a charge sensitive preamplifier used with a solid-state radiation detector. These signals typically have (1) a small amplitude, in the range of a few mV, (2) a fast rise (tens of nsec to  $\mu$ sec), and (3) following the signal, either a slow decay (of order msec) or no decay. A charge sensitive preamplifier integrates the current into its input, so over time the output drifts towards the rail. One of two methods is usually used to restore the output.

Some preamplifiers use a pulsed reset to periodically restore the input charge. In such preamps, there is no tail after the signal. A radiation interaction generates a voltage step, then the output is constant until the next step, as illustrated in Figure 2(a). Eventually, the output will drift near the supply rail and is then reset to its initial value, leading to a very large and fast reset signal. The DP4 is configured from the factory for use with such reset-type preamplifiers. The reset results in a large, negative going pulse into the ADC, which disrupts the signal processing. The preamplifier output can take a significant time to fully recover from a reset. Pulses received during reset recovery will have a distorted amplitude and degrade the spectrum. Therefore the DP4 includes hardware to lock out data acquisition during reset.

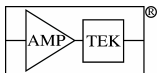


(a)



(b)

Figure 2. Oscilloscope traces showing typical preamplifier outputs, for reset (a) and continuous (b) preamplifiers. The DP4 is shipped from the factory configured for the reset inputs, such as those on the left.



Some preamplifiers use a continuous feedback, the simplest of which is a resistor in parallel with the feedback capacitor. After the voltage step due to each signal interaction, the output slowly drifts back to its quiescent value, with the time constant of the feedback, as illustrated in Figure 2(b). This time constant is long, 500  $\mu$ sec in this case, so that the charge in the signal can be accurately integrated. The DP4 hardware may be configured for use with most continuous feedback preamplifiers. This is discussed in Section 0

### 1.3 PULSE SHAPING AND SELECTION

#### 1.3.1 Pulse Shaping

The DP4 implements trapezoidal pulse shaping, with a typical output pulse shape shown in Figure 3. This shape was chosen because it provides a near optimum signal to noise ratio for many detectors, including Amptek's XR100 detectors under normal operating conditions. The user can adjust the rise/fall time (the rise and fall must be equal) and the duration of the flat top. These values can be set to a large number of discrete values, shown in Table 1.

A semi-gaussian amplifier with shaping time  $\tau$  has a peaking time of  $2.2\tau$  and is comparable in performance with the trapezoidal shape of the same peaking time. So, if the DP4's digital shaper were to be set to the equivalent of an analog amplifier with a 12  $\mu$ s shaping time constant it would be set to roughly  $2.2 \times 12 = 26.4 \mu$ s peaking time.

The electronic noise of a detector will generally have a minimum at some peaking time, the "noise corner." At peaking times shorter or longer than this, there is more noise and hence degraded resolution. If this peaking time is long relative to the rate of incoming counts, then pulse pile-up will occur. In general, a detector should be operated at a peaking time at the noise corner, or below the noise corner as necessary to accommodate higher count rates.

If the risetime from the preamp is long compared with this peaking time, then the output pulses will be distorted by ballistic deficit. In this case, the trapezoidal flat top can be extended to improve the spectrum. The specific optimum timing characteristics will vary from one type of detector to the next and on the details of a particular application, e.g. the incoming count rate. The user is encouraged to test the variation of performance on these characteristics.

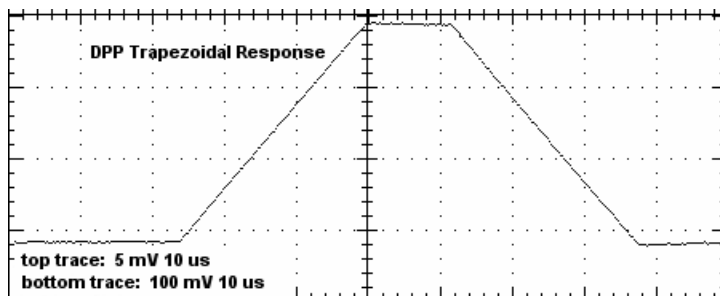
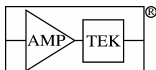


Figure 3. Pulse shape produced by the DP4.



Peaking Time (uS)	Flat Top (uS)	Decimation	'Rise' register	Flat Top register	Decimation register
0.8	0.2...3.2	1	1	0...15	0
1.6	0.2...3.2	1	2	0...15	0
2.4	0.2...3.2	1	3	0...15	0
3.2	0.2...3.2	1	4	0...15	0
4.0	0.2...3.2	1	5	0...15	0
4.8	0.2...3.2	1	6	0...15	0
5.6	0.2...3.2	1	7	0...15	0
6.4	0.2...3.2	1	8	0...15	0
8.0	0.4...6.4	2	5	0...15	1
9.6	0.4...6.4	2	6	0...15	1
11.2	0.4...6.4	2	7	0...15	1
12.8	0.4...6.4	2	8	0...15	1
16.0	0.8...12.8	4	5	0...15	2
19.2	0.8...12.8	4	6	0...15	2
22.4	0.8...12.8	4	7	0...15	2
25.6	0.8...12.8	4	8	0...15	2
32.0	1.6...25.6	8	5	0...15	3
38.4	1.6...25.6	8	6	0...15	3
44.8	1.6...25.6	8	7	0...15	3
51.2	1.6...25.6	8	8	0...15	3
64.0	3.2...51.2	16	5	0...15	4
76.8	3.2...51.2	16	6	0...15	4
89.6	3.2...51.2	16	7	0...15	4
102.4	3.2...51.2	16	8	0...15	4

Table 1. Table of allowed rise/fall times (peaking times) and flat top times.

The pulse shaping of the DP4 is illustrated in Figure 4. The top trace shows the input to the DP4, which is the output from a reset-type charge sensitive preamplifier. This is processed by the analog prefilter (see Figure 1), producing the prefilter output shown at the bottom. This is digitized and then processed digitally, producing the DP4's shaped output, also shown at the bottom.

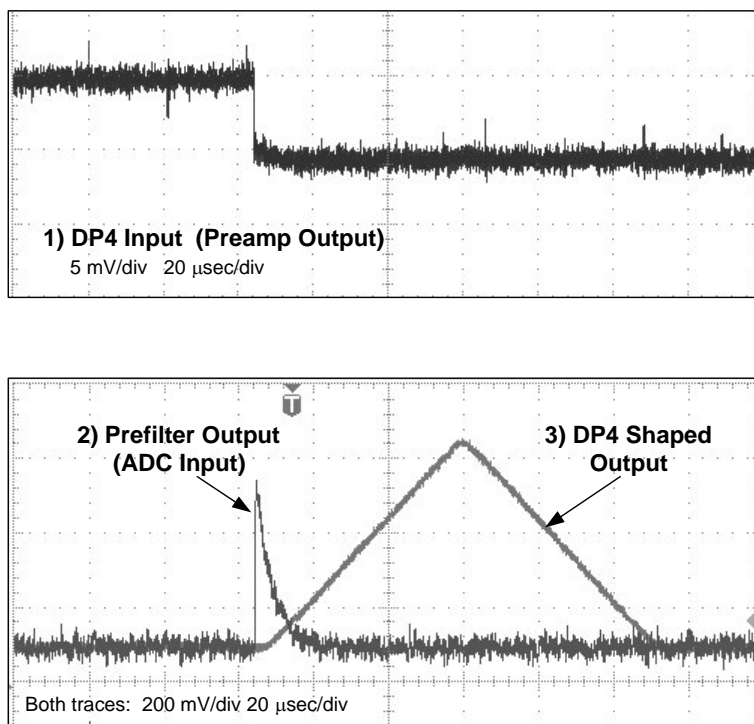
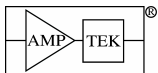


Figure 4. Oscilloscope trace illustrating the normal operation of a DP4.



### 1.3.2 Baseline Restoration (BLR)

The “baseline” of a digital processor has some significant differences from traditional analog shaping amplifiers. Traditional amplifiers generally include some form of baseline restoration, DC feedback, to prevent drift at high count rates. Because the DP4’s transfer function has a finite impulse response, after a pulse has passed through the processing pipeline it has no impact on the output. This is fundamentally different from an analog differentiator and results in vastly enhanced baseline stability at high count rates. However, unlike analog shapers the DP4 has to establish a DC baseline, at all count rates. There are two options available in the DP4 to establish the DC baseline: “auto-baseline”, which involves measuring the input offset, and baseline restoration, which uses closed loop, quasi-DC feedback.

#### 1.3.2.1 Auto-Baseline

The ‘Auto-Baseline’ function does not correct baseline variations resulting from count-rate changes or other detector effects; rather, it corrects for drift in the DP4’s analog section, due mostly to temperature changes. It is intended to be used with reset-style preamps that do not otherwise require BLR (i.e. the Amptek XR100CR). When the DP4 detects that reset has occurred, it temporarily disconnects the detector from the DP4 front-end electronics and averages the voltage offset produced by the front end. The detector is reconnected and the measured offset is used to correct the digital baseline. This doesn’t affect throughput since the processing is suspended anyway during reset to allow the preamp signal to settle.

#### 1.3.2.2 BLR

The DP4 also has an asymmetric baseline restorer, which can be used when baseline shifts due to count-rate changes, power supply drift, or if other detector effects need to be nulled. It works as follows:

- a. All digital samples below the existing baseline are integrated. When the sum reaches a preset value (the “BLR Correction Threshold”), an upward correction (the “Baseline Up Correction”) is added to the baseline.
- b. Countering this occasional upward correction is a periodic downward correction (the “Baseline Down Correction.”)

As the magnitude of these corrections is typically much less than one channel, the periodic downward correction and occasional upward correction should not adversely affect resolution. Each of the corrections has four settings (very slow, slow, medium and fast) and the correction threshold also has four settings (very fast, fast, normal and slow.) It should be noted that the relative size of these corrections is dependent on peaking time; thus a setting that works well at a particular peaking time may not necessarily be ideal for a different peaking time.

BLR and Auto-Baseline should not be used at the same time.

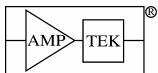
### 1.3.3 Pulse Selection

#### 1.3.3.1 Pile-Up Rejection

The goal of the pile-up reject (PUR) logic is to determine if two interactions occurred so close together in time that they appear as a single output pulse with a distorted amplitude. The DP4 PUR uses a “fast-slow” system, in which the pulses are processed by a fast shaping channel in parallel with the slower main channel (both channels are purely digital). Though similar in principle to the techniques of an analog shaper, the pile-up reject circuitry and the dead time of the DP4 differ in significant ways, resulting in much better performance at high count rates. First, the symmetry of the shaped pulse permits the dead time and pile-up interval to be much shorter. Second, there is no dead time associated with peak acquisition and digitization, only that due to the pulse shaping. [Setting 0 = off].

Figure 5 illustrates the operation of the DP4 for pulses that occur close in time. Figure 5 (a) shows two events that are separated by less than the rise time of the shaped signal, while Figure 5 (b) shows two pulses that are separated by slightly longer than the rise time. In (a), the output is the sum of the two signals (note that the signal amplitude is larger than the individual events in (b)) and the events are said to be piled up. However, note that the analog prefilter outputs in (a) are separate. For a nearly triangular shape, pile-up only occurs if the two events are separated by less than the peaking time, in which case a single peak is observed for the two events. The interval used by the DP4 for both dead time and pile-up rejection is the





sum of risetime, plus about 20% of the risetime to account for jitter, and the flat-top duration. If two events occur within this interval and pile-up rejection is disabled, then only the single, piled-up value is in the spectrum. If pile-up rejection is enabled and two events are separated by more than the fast channel pulse pair resolution (600 nsec) and less than this interval, both are rejected. Events that exceed a threshold in the fast channel trigger the pile-up reject logic.

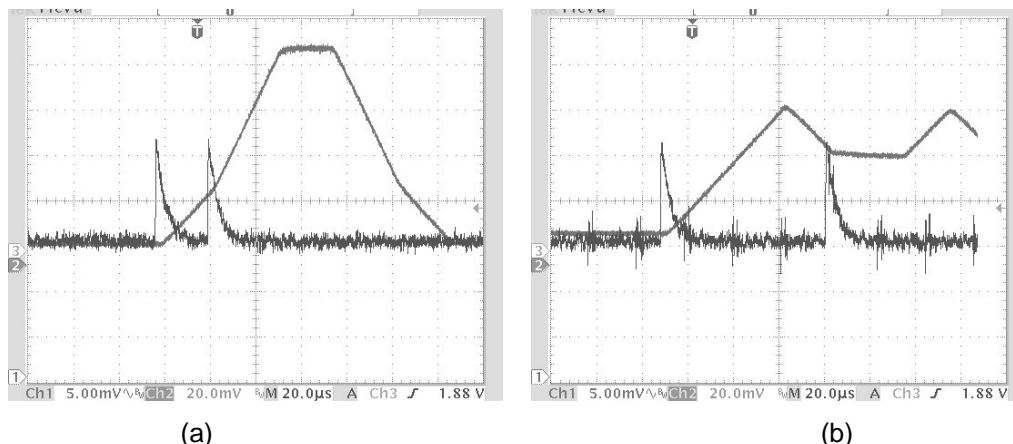


Figure 5. Oscilloscope traces illustrating the dead time and pile-up reject performance of the DP4

### 1.3.3.2 Risetime Discrimination

In some types of detectors, pulses with a slow risetime have a charge amplitude deficit. For example, in many diodes there is an undepleted region with a weak electric field. A radiation interaction in this region will generate a signal current, but the charge motion is slow through the undepleted region. This leads to a slow rising edge on the pulse and since charges are trapped, a small pulse. Interactions in this region can lead to various spectral distortions: background counts, shadow peaks, asymmetric peaks, etc. In risetime discrimination, events with a slow rise do not contribute to the spectrum but are rejected.

The DP4 implements RTD by measuring the width of the fast channel response: a slower input rise time leads to a broader fast channel output. Because a broader fast channel output also has a lower amplitude (to maintain the same net area), the DP4 measures the Half-Width, Half-Max (HWHM) of the resulting response. This measured width is compared to a preset width (the "RTD Time Threshold") and the event is rejected if the measured width is too wide. [Note that the event can only be rejected if the Fast Channel is over threshold. See the next section for a discussion of thresholds.]

Because the fast channel is inherently much noisier than the slower shaped channel, an RTD threshold is also implemented on the shaped channel. Events which fall below this threshold (the "RTD Slow Threshold") are not processed by the RTD and are thus accepted (unless otherwise rejected by Pileup Rejection or some other criterion). Because RTD is most often needed on interactions deep in a detector, arising from high-energy events, low-amplitude events are unlikely to benefit from RTD rejection. These fall below the RTD Slow Threshold and are thus accepted.

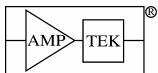
To summarize the RTD rules:

- Events whose shaped (slow) channel amplitude is below the RTD Slow Threshold are kept; otherwise...
- Events whose fast channel amplitude is below the fast threshold are rejected; otherwise...
- Events whose measured HWHM is wider than the RTD Time Threshold are rejected.

### 1.3.3.3 Thresholds

**Slow channel threshold:** The DP4 uses the Slow Channel Threshold to distinguish between events that should be added to the stored spectrum and those that shouldn't. Events with an amplitude lower than the Slow Channel Threshold are ignored – they do not contribute to the stored spectrum. The slow channel threshold is the equivalent of a low-level discriminator (LLD).





**Fast Channel Threshold:** The Fast Channel Threshold is used for two functions: Rise Time Discrimination (RTD), as described in section 1.3.3.2, and Pile-up Rejection (PUR). The DP4 can only reject piled-up events if both events fired the fast channel; therefore, it is usually desirable to set the Fast Channel Threshold as close to the noise as is practical. This is discussed in more detail in later sections. If RTD and PUR are not used, then the fast channel threshold is not important.

#### 1.3.3.4 Gate

The gate input is used with external circuitry to determine if events should be included or excluded from the spectrum. The gate can be active high or active low (or disabled). If disabled, then this input is ignored and all events (which meet the criteria above) are counted. If active high (low), then if the gate input is high (low), the event is counted in the spectrum. When counts are gated off, the clock is also gated off so that an accurate count rate can be determined.

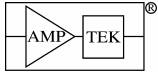
The timing of this gate input is important. If the gate input is active while the fast channel threshold is triggered, then the event is counted as a fast count. If the gate input is active when the peak detect is triggered, then the event is counted as a slow count and shows up in the spectrum. Note that the fast and slow channels are triggered at different times, since they have different shaping times. We recommend that the gate input duration be equal to or greater than the sum of the peaking and flat top durations.

#### 1.3.4 Multichannel Analyzer

The MCA portion of the DP4 supports 256, 512, 1024, 2048, 4096 or 8192 channels. (8192 channels is only available via the USB interface – it is not supported via RS232.) The DP4 uses 3 bytes per channel, which allows up to 16.7M counts per channel. The MCA has two spectral buffers available, A and B, which can be selected either via software, or by a hardware signal.

#### 1.3.5 Single Channel Analyzer

The DP4 contains eight single channel analyzers (SCAs). Each SCA has an upper and a lower threshold. If an event occurs with a shaped output within the range defined by these thresholds, then a logic pulse is generated and is output to the JP9 connector on the DP4, where it can be connected to external hardware. The upper and lower limits of the 8 SCAs can be set independently in the software. SCA8 serves a dual purpose – not only does it operate like the other SCAs, but it is also used to set the Region-of-Interest (ROI) for the Preset Count mode of MCA operation. That is, when a Preset Count is selected, the MCA will stop after the programmed number of counts occurs in the SCA8 ROI.



## 1.4 DP4 INTERFACE

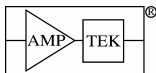
There are two distinct components to the DP4 software. The microcontroller on the DP4 contains embedded software that controls data acquisition and the interface. The computer to which the DP4 interfaces must contain software to communicate via the serial port (USB or RS-232). The current revision of the DP4 is designed primarily for use in OEM applications, embedded in an end-user's product. As such, the user may access the embedded software to tune the instrument for his/her application. Further, the personal computer software that is supplied is essentially a demonstration program. It permits the user to fully access the DP4 functionality and can be used as is, but more importantly it shows how to carry out the various functions. We presume that the user will tailor this software to meet the specific requirements of his/her application.

The DP4 has both a USB interface and a standard RS232 interface. Specifically, it has a full-speed (12Mbps) USB 1.1 interface (which is also compatible with newer USB 2.0 ports.) Amptek has licensed a USB device driver for use with Windows 98, Windows ME, Windows NT, Windows 2000 and Windows XP, which makes it easy to write Windows software to communicate with the DP4.

### **Note on the USB device driver**

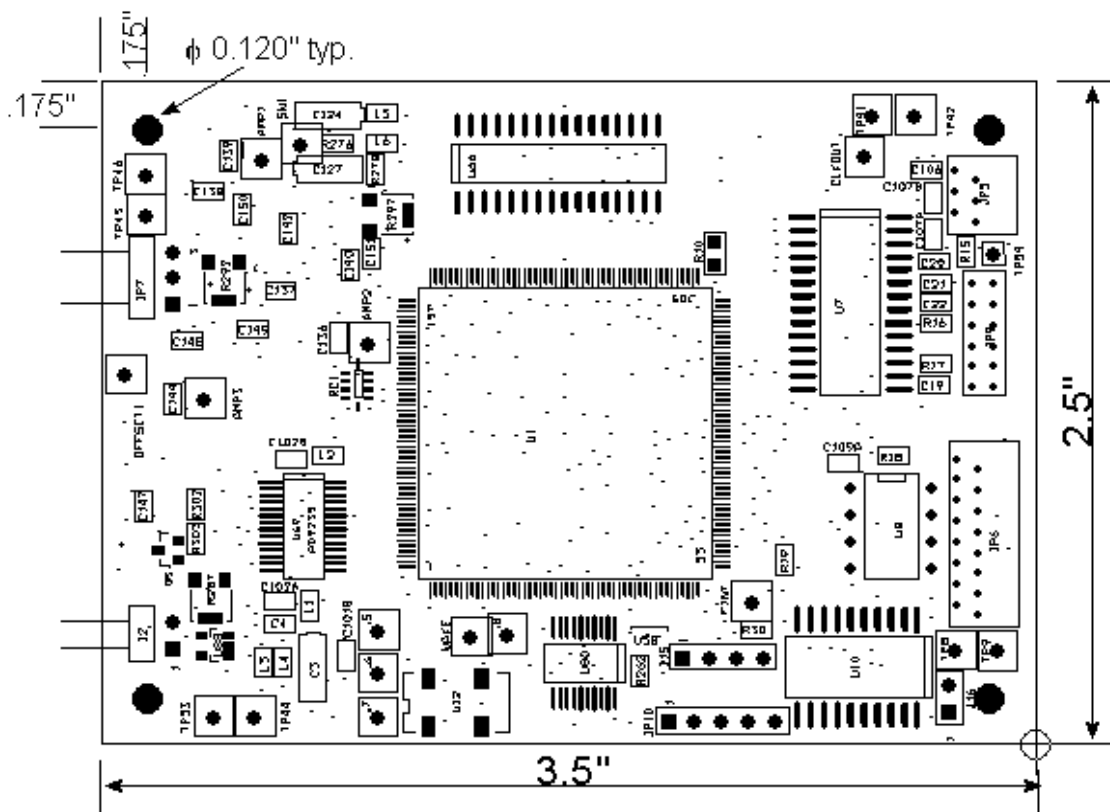
*The USB device driver is licensed from Andrew Pargeter & Associates ([www.devicedriver.com](http://www.devicedriver.com)) for the Amptek DP4. The license agreement allows Amptek to provide the driver to the OEM, and the OEM to provide the driver to the end user provided that the embedded code doesn't change. In practice, an OEM who wishes to write his own embedded code will either need to relicense the USB driver or find another driver solution. If the OEM wishes only minor changes to the existing embedded code, he should contact Amptek to see if the changes could be made to the standard code, and thus would be covered by the license agreement.*

*The USB Vendor ID (VID) and Product ID (PID) are provided to Amptek from Andrew Pargeter & Associates ("APA") as part of the license agreement. The VID (0x0BD7) is owned by APA, and the PID (0xA021) is licensed for use only with the Amptek DP4. OEMs may not use this VID/PID combination, except with the standard Amptek DP4 embedded code. Contact Amptek for more information. For more information on VIDs & PIDs, refer to the USB Implementer's Forum ([www.usb.org](http://www.usb.org)).*



## 2 DP4 SPECIFICATIONS

### 2.1 DIMENSIONS



### 2.2 CONNECTIONS

There are two primary connectors, which are necessary for the DP4's operation, along with some auxiliary connectors. JP7 is the analog input, which connects to a preamplifier output. JP6 contains the power supply connections and the serial interface. These are the primary connectors and are required for operation. Their use is shown graphically in Figure 6.

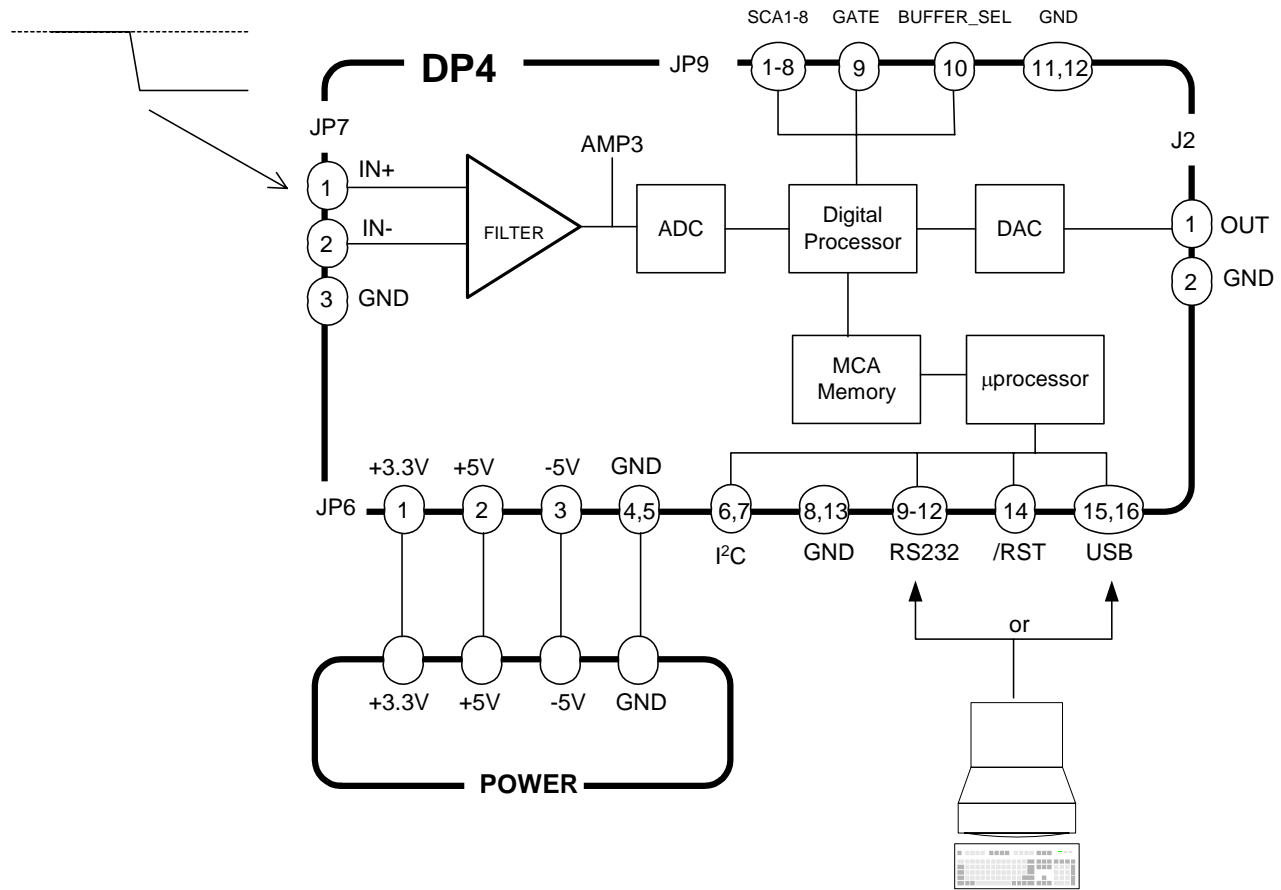
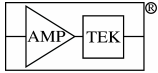


Figure 6. Block diagram illustrating the primary connections.

The auxiliary connectors include (1) an analog output, the output of a DAC, J2; (2) a proprietary test connector, JP5; (3) an external I/O connector with SCAs, GATE and BUFFER\_SEL, JP9; and (4) a user connector, JP10, which is tied to four microcontroller pins.

### 2.2.1 JP7 – Analog input

This is the input to the DP4 from a preamplifier. +IN and –IN form a differential input to the DP4, which is an inverting amplifier.

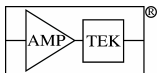
- Pin 1: +IN: Non-inverting input. For negative pulses, connect signal to +IN and return to –IN.
- Pin 2: –IN: Inverting input. For positive-going pulses, connect signal to –IN and return to +IN.
- Pin 3: AGND: Analog ground.

Connector:

- The JP7 connector on the DP4 is a Molex P/N 22-05-3031. Mating connector is: Molex P/N 22-01-3037 (Digi-Key P/N WM2001-ND) with Molex crimp terminals P/N 08-50-0114 (Digi-Key P/N WM1114-ND).

Requirements:

- Polarity: The DP4 is an inverting amplifier. Measured at Pin 1 referenced to Pin 2, the input pulse should be negative. The connector should be wired to achieve this as discussed above.
- Magnitude: The inputs to the first amplifier stage have a common mode range of  $\pm 7.6V$ , with a differential mode range of  $\pm 3.8V$ . By default, a 25% attenuator is installed ( $R_{291}=R_{296}=330\text{ ohms}$ ) to increase the common mode range to  $\pm 9.5V$  and the differential mode range to  $\pm 4.75V$ . If this increased range isn't needed, the attenuator can be removed ( $R_{291}=R_{296}=0\text{ ohms}$ ). See section 2.3.1.



- The default configuration is for reset preamps. For continuous feedback preamplifiers, the hardware will require reconfiguration, as discussed in Section 0.
- Risetime >100 nsec

### 2.2.2 JP6 – Power and Interface

JP6 is a 16-pin 1mm flex connector.

Pin #	Name	Pin #	Name
1	+3.3V	9	RS232-RX
2	+5V	10	RS232-TX
3	-5V	11	RS232-CTS
4	GND	12	RS232-RTS
5	GND	13	GND
6	I <sup>2</sup> C SDA	14	/RESET
7	I <sup>2</sup> C SCL	15	USB-
8	GND	16	USB+

Table 2. Pinout for JP6, the primary power and serial interface connector

- +3.3V: This supply powers the majority of the DP4. Average operating current is 100-200mA, depending on configuration. Peak current is 500 mA at startup.
- +5V, -5V: These supplies power the analog front end. Average operating current is 10 mA for each. These should be well filtered, since ripple is likely to degrade performance. There is no overcurrent or reverse voltage protection implemented on the DP4.
- SDA, SCL: These are the I<sup>2</sup>C bus signals. The DP4 microcontroller is the bus master, so any peripherals connected to the I<sup>2</sup>C bus must be slaves. The only I<sup>2</sup>C devices on the DP4 (other than the  $\mu$ C) are the 24AA64 boot prom and a temperature sensor.
- RS232-RX, RS232-TX, RS232-CTS, RS232-RTS: These are RS232 signals for interfacing the DP4 to a host system. The signal names are relative to the DP4, i.e. the DP4 receives on the RX pin and transmits on the TX pin. The handshaking signals CTS and RTS are not used but are available for custom applications.
- /RESET: Pulling this signal low will hold the entire DP4 in reset. Floating it or pulling it high allows normal operation.
- USB+, USB-: This is the USB (Universal Serial Bus) communication bus. The DP4 microcontroller contains a USB communication core.

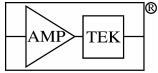
Connector:

- Connector: 16 position right angle, Hirose Electronic Co. Ltd: FH21-16S-1DS, Digi-Key: HFG16T-ND
- Mating cable: 1mm Flat Flex Cable 4", Parlex: 100-16-102B, Digi-Key: HF16U-04-ND (other lengths are available)

### 2.2.3 J2 – Analog output

This is the shaped output from the DAC. The decimated input and other diagnostic signals can also be output from the DAC.

- Pin 1: +OUT: This is the output of the DAC. Output range is 0-1V.



- Pin 2: AGND: Analog ground. Care should be taken in connecting this ground externally, as ground currents can disturb the analog front end.

Connector:

- The J2 connector on the DP4 is a Molex P/N 22-05-3021. Mating connector is: Molex P/N 22-01-3027. (Digi-Key P/N WM2000-ND) with Molex crimp terminals P/N 08-50-0114 (Digi-Key P/N WM1114-ND)

#### 2.2.4 JP9 External Logic I/O

JP9 is an 8x2 2mm header, which offers functionality which is required by some but not all users. Pins 1 through 8 are the outputs of the single channel analyzer outputs, discussed in section 1.3.5. Pins 9 and 10 are the gate input (section 1.3.3.4) and buffer select input (section 2.3.4), respectively. Pins 11 and 12 are ground.

Pin	Function	Pin	Function	Pin	Function
1	SCA1	5	SCA3	9	GATE IN
2	SCA8	6	SCA6	10	BUFFER SEL
3	SCA2	7	SCA4	11	GND
4	SCA7	8	SCA5	12	GND

GATE and BUFFER\_SEL inputs:

$V_{IL}$  (logic low): -0.5 to + 0.7V

$V_{IH}$  (logic high): +2.4 to +5.5V

Inputs: SN74LVC2G14,  $V_{cc}$ =3.3V, 100 k $\Omega$  pull-downs

SCA Outputs:

$V_{OL}$  (logic low): 0.1V @ 100uA

$V_{OH}$  (logic high): +3.1V @ 100uA

Outputs: SN74LVC245A,  $V_{cc}$ =3.3V, 49.9  $\Omega$  series termination

Pulse width: 50nS

#### 2.2.5 J15 I<sup>2</sup>C Bus

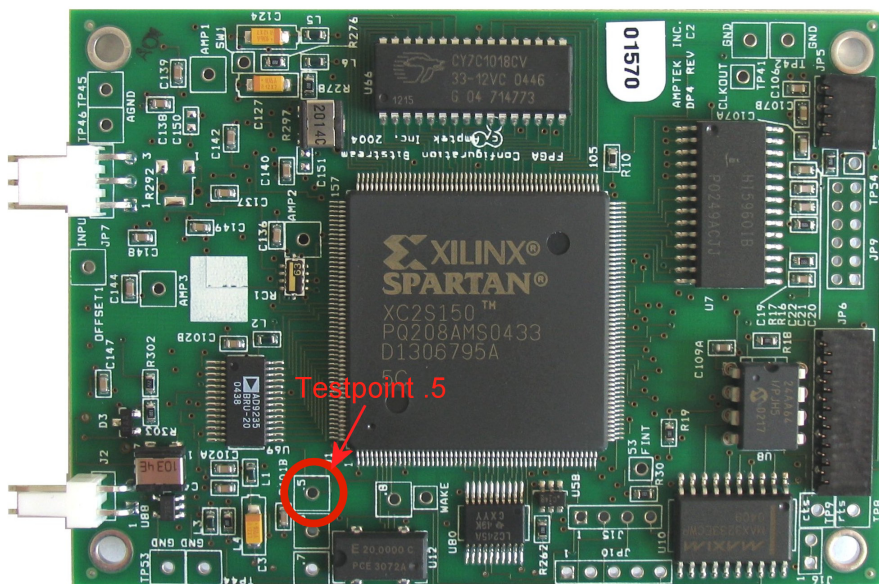
J15 includes the I<sup>2</sup>C bus signals (SCL & SDA), and a global active low reset input (/RESET). This header can be used for in-circuit programming of the microcontroller EEPROM, or it can be used by custom applications to communicate with other I<sup>2</sup>C devices.

#### 2.2.6 Diagnostic Testpoint .5

The DP4 has a diagnostic testpoint, labeled '.5', which is located near the FPGA (see picture below). This testpoint can be configured via the application software to output a number of useful signals, as listed below:

Signal Name	Function
ICR	Input Count Rate, i.e. Fast Channel fired
PILEUP	Piled-up event detected
HOLD	(Internal diagnostic)
ONESHOT	Period during which a 2nd event would be considered piled-up
DET_RES_	Active-Low Detector Reset Lockout Period

MCA_EN	High=MCA Enabled, Low=MCA Disabled
TRIGGER	Peak Detect Fired
SCA8	Single Channel Analyzer output #8 (Also available on JP9)



## 2.2.7 JP10 Extra signals for OEM use

JP10 contains signals from four unused pins on the microcontroller. These pins are configured as outputs, and can be controlled via USB commands (See section 5.2.1). The outputs go between 0V (0.4V @ -1.6mA) and +3.3V (+2.4V @ 1.6mA).

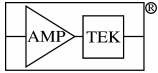
Pin #	Function
1	Output #1
2	Output #2
3	Output #3
4	Output #4
5	GND

## 2.3 CONTROLS AND ADJUSTMENTS

### 2.3.1 Analog Prefilter

- Inversion: On JP7, pins +IN and -IN form a differential input. The DP4 requires a negative pulse on +IN relative to -IN.
- Input Attenuation: If the signal exceeds the nominal range of +/- 3.8V, R291 & R296 can be used to attenuate the input signal. R291=R296=330 ohms yields 25% attenuation (the default configuration); 1Kohm yields 50% attenuation.

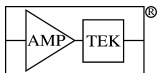




- **Coarse Gain:** Four coarse gain settings are available, by command from the microcontroller. The gain settings are x10.8, x20.7, x55.4, and x106.2.
- **Fine Gain:** Fine gain is adjusted digitally, via software, over a range of +/- 25%.
- **Offset:** The pot R287 sets the DC offset into the ADC. The ADC input should never drop below zero, or significant distortions in the pulse shape will occur.
- **Input Pole:** The pot R297 is used to set an input pole, part of the prefilter function.

### 2.3.2 Pulse Shaping

- **Rise and Fall Time:** The rise time of the shaped pulse, which must equal the fall time, can be set to any one of several values, listed in Table 1. This is adjusted digitally: the microcontroller writes the desired value to a register in the pulse shaping hardware. The demonstration software provides a simple control for this. Setting this value by the demonstration software is described in sections 3.2.2 and 4.
- **Flat Top Duration:** The duration of the trapezoidal flat top can also be set to one of several values, by a digital command.
- **Decimation:** For long rise times, the input ADC values are decimated, as is common with digital processing. The decimation setting is related to the rise/fall time and the flat top duration. This is also set by digital command.
- **DAC Controls:** The DAC has several controls, described more fully in section 5. The DAC provides an analog display of the digital processing that is occurring. The analog display is not needed but is convenient for setup and debugging. First, the DAC can be enabled or disabled. Second, several different waveforms may be sent to the DAC. This includes the fast channel output, the decimated input, the shaped output, and the BLR correction. Third, a DC offset can be sent to the DAC. The DAC responds to underflows (outputs below 0V) by wrapping over, so it is recommended practice to set a DC offset that avoids this.
- **Preamp Reset Controls:** These are utilized with reset type preamps and their operation is described in section 1.3.2.1. The user may enable or disable Autobaseline. The user may also set a reset period, which is the length of time following a reset signal during which data processing is shut down, to permit the electronics to fully recover. The user may also elect to disable reset detection. These controls are sent by software to the pulse processing FPGA.
- **Baseline Restoration Controls:** The operation of the baseline restorer is described in section 1.3.2.2. The user may enable or disable BLR. If enabled, then the user may choose to set three parameters: up, down, and threshold, each set to one of four values. "Up" ("Down") determines the size of the upward (downward) step to the baseline. "Threshold" determines when an upward correction is required. These controls are sent by software to the pulse processing FPGA. Autobaseline should be disabled if BLR is enabled or if a non-reset style preamp is used.



### 2.3.3 Pulse Selection

- **Fast Threshold:** A low level threshold for the fast channel can be set by a digital command. The logic output is used in subsequent pulse processing.
- **Pile-Up Rejection:** The pile-up rejection (PUR) has one direct control, the on/off control. Indirectly, the operation of the PUR is greatly affected by the setting of the Fast Channel Threshold. Only signals with a fast channel response exceeding this threshold are evaluated for possible pile-up. If this threshold is set too low, then electronic noise triggers the PUR detect circuits. Pulses are rejected if they occur close in time with noise, and therefore there is very low data throughput. If this threshold is set too high, then real events are missed and therefore pile-up will be present in the spectrum. Common practice is to set the fast threshold to generate 5-10 cps, in the absence of any signal, which puts this level as close to the noise as possible without degrading throughput.
- **Pile-up period:** the pile-up period (the minimum interval between two successive peaks which are not considered piled up) is programmable. The optimal setting is:

$$(\text{RisetimeRegister} * 19 + (\text{FlatTopRegister} + 1) * 4) / 2.$$

- **Risetime Discrimination:** Risetime discrimination is described in section 1.3.3.2. There are three controls, each sent via software to the FPGA. First, RTD may be enabled or disabled. Second, if enabled, then the user may set the threshold. This threshold applies to the slow channel. Only events exceeding this threshold will be analyzed by the RTD circuit; all events below this threshold are accepted. Third, the user may set the HWHM for the fast channel. Only events with a HWHM below this value will be accepted.

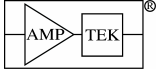
### 2.3.4 MCA Control

- **Number of channels:** The MCA can be set to have 256, 512, 1024, 2048, 4096, or 8192 channels.
- **Slow Channel Threshold (LLD):** As with most MCAs, there is a low level discriminator on the slow channel. Only pulses exceeding this threshold will be recorded in the MCA spectrum. The register setting of 0-255 corresponds to about 0-25% of the full-scale output.
- **Gate:** In software, the user may set the gate "off", in which case the gate input is ignored. The user may also set it to active high or active low.
- **Buffer:** There are two memory buffers in the hardware, designated A and B. The user may choose to use either. In addition, the user may choose to enable "Hardware Select". If this is enabled, then an external logic input controls whether the data go into buffer A or B.
- **Preset Time:** The accumulation time may be preset, from 100ms to 19.4 days, with 100ms precision. This is set in software. After this time has elapsed, acquisition will stop. This will be the accumulation time, the duration of data acquisition, not live time and not elapsed clock time. See section 7.3 for details on accumulation time.
- **Preset Counts:** The DP4 can be programmed to acquire a preset number of counts in a region of interest. Acquisition will stop when this number of counts is reached. SCA8 must be configured with the region of interest.

### 2.3.5 SCA Controls

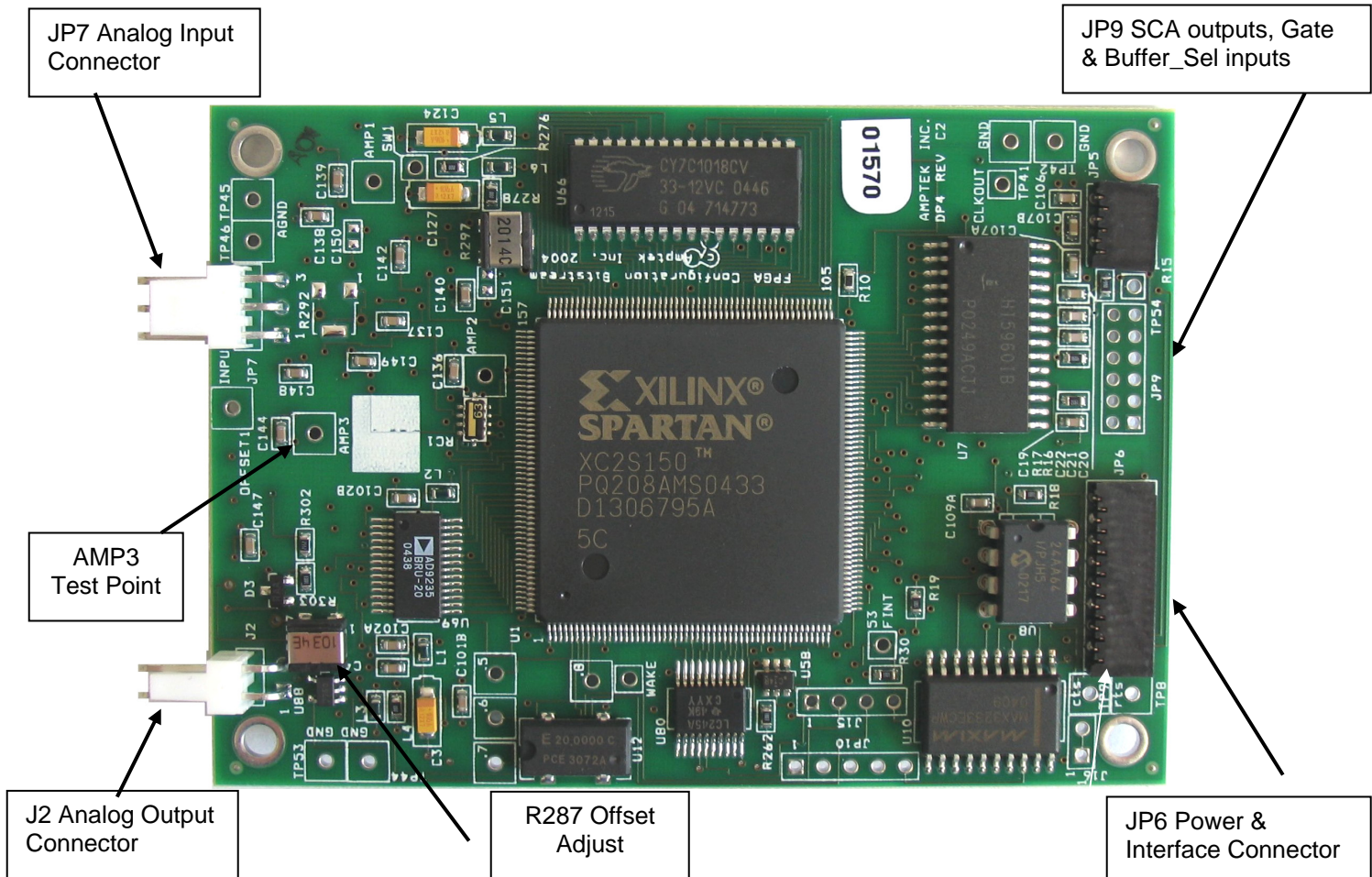
There are 8 SCA channels, each of which has the following three controls.

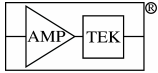
- **Enable:** If this is selected, then that channel outputs counts.
- **Lower and Upper Thresholds:** These define the range of the SCA. These are in MCA channels: if the MCA is in 1024 channel mode, and SCA 1 has a range of 712 to 800 for example, then any time a count is binned in this range of MCA channels, there will be a logic pulse on the SCA output.



### 3 QUICK START INSTRUCTIONS

The purpose of this section is to provide enough information to set up the DP4 hardware, install the demonstration software, and start taking data. More detailed information on the hardware and software is elsewhere. In particular, the interface software which runs on the personal computer is described in more detail in section 4. The most important connectors and controls are shown below.





### 3.1 SET-UP INSTRUCTIONS

#### 3.1.1 Software installation and serial port connection (USB)

- 1) All of the necessary software is on the CDROM. Run the 'setup' program in the DP4 folder to install the compiled Visual Basic software. [The Visual Basic source code is in the 'Source Code\VB' folder]
- 2) Connect the USB interface, per section 2.2.2 on page 13, to the USB port of a personal computer or hub. [A USB 'A' to 'B' cable is required to connect between the USB connector on the optional DP4 connector or power supply boards (PC4-1,2,3) and the USB port of a PC or hub.] Apply power to the DP4; the 'New Hardware Wizard' should automatically start on the PC. Follow the directions below to install the USB device driver, depending on which version of Windows is in use.
- 3) For Windows 2000 or Windows XP:
  - a. In the "Found New Hardware Wizard" (which should automatically appear when the DP4 is connected and powered on for the first time), select "Install from a list or specific location", and click "Next >".
  - b. Select "Don't Search. I will choose the driver to install." and click "Next >".
  - c. Click the "Have Disk..." button.
  - d. Select "Browse..." and navigate to the \USB\_driver\Win2K\_XP folder of the DP4 CDROM. Select "OK".
  - e. Click "Next >".
  - f. Click "Finish". The USB driver should now be installed.
- 4) For Windows 98 or Windows ME:
  - a. The "Add New Hardware Wizard" should automatically appear when the DP4 is connected and powered on for the first time. Click "Next >".
  - b. Select "Search for the best driver for you device" and click "Next >".
  - c. Select only "Specify a location:", click "Browse" and navigate to the \USB\_driver\Win98\_ME folder of the DP4 CDROM. Click "Next >".
  - d. Windows is now ready to install the driver. Click "Next >".
  - e. Click "Finish". The USB driver should now be installed.

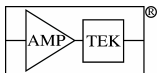
*Note for users of the original DP4: The original DP4 only supported up to 4096 channel spectra, and therefore the USB driver was configured to not allow transfers larger than that. The DP4 Rev. C now supports 8192 channel spectra, which may not work properly with the previous driver configuration if the DP4 is configured for 8192 channels. There are 2 solutions: 1) Uninstall the USB driver, and reinstall as described above. 2) Edit the registry entry which limits the transfer size to 4096 channels. Please contact Amptek for guidance if this issue affects you.*

#### 3.1.2 Software installation and serial port connection (RS232)

- 1) All of the necessary software is on the CDROM. Run the 'setup' program in the DP4 folder to install the compiled Visual Basic software. [The Visual Basic source code is in the 'Source Code\VB' folder]
- 2) Connect the RS232 interface, per section 2.2.2 on page 13, to the serial port of a personal computer. The RS232 handshaking lines RTS & CTS don't need to be connected unless custom software is used. Amptek offers several different DP4 power supply solutions (PC4 interface boards) which include standard RS232 connectors.

#### 3.1.3 Hardware connections

- 1) Connect the power supply and the RS232 or USB interface, per section 2.2.2 on page 13. The +3.3V, +/-5V, GND, and RS232 or USB lines must be connected. We recommend verifying the voltages and current limits of the power supply before connecting to the DP4. The RS232 lines should connect to the



serial port of a personal computer; the USB lines can connect to the USB port of a PC or to a USB hub. [The RS232 handshaking lines RTS & CTS don't need to be connected unless custom software is used.]

- 2) Connect the preamplifier output to the DP4 input JP7, per section 2.2.1 on page 12.
- 3) Connect the DP4 analog output J2, per section 2.2.3 on page 13, to an oscilloscope. Although this output from the DAC is not required for operation, it is recommended during initial set up. Use jumper pins 1 and 2 of JP8 to enable the DAC.

### 3.1.4 Power On

- 1) Turn on the detector and preamplifier and place an appropriate radioactive source in front of the detector. It may be useful to verify, using an oscilloscope, that the preamplifier is producing signals of the correct size and polarity.
- 2) With the computer on, double click on the PX4.EXE icon. The screen should look as below. The CONFIGURE button will be yellow when the user has made changes to the configuration on the screen but not yet sent the new configuration to the DP4.

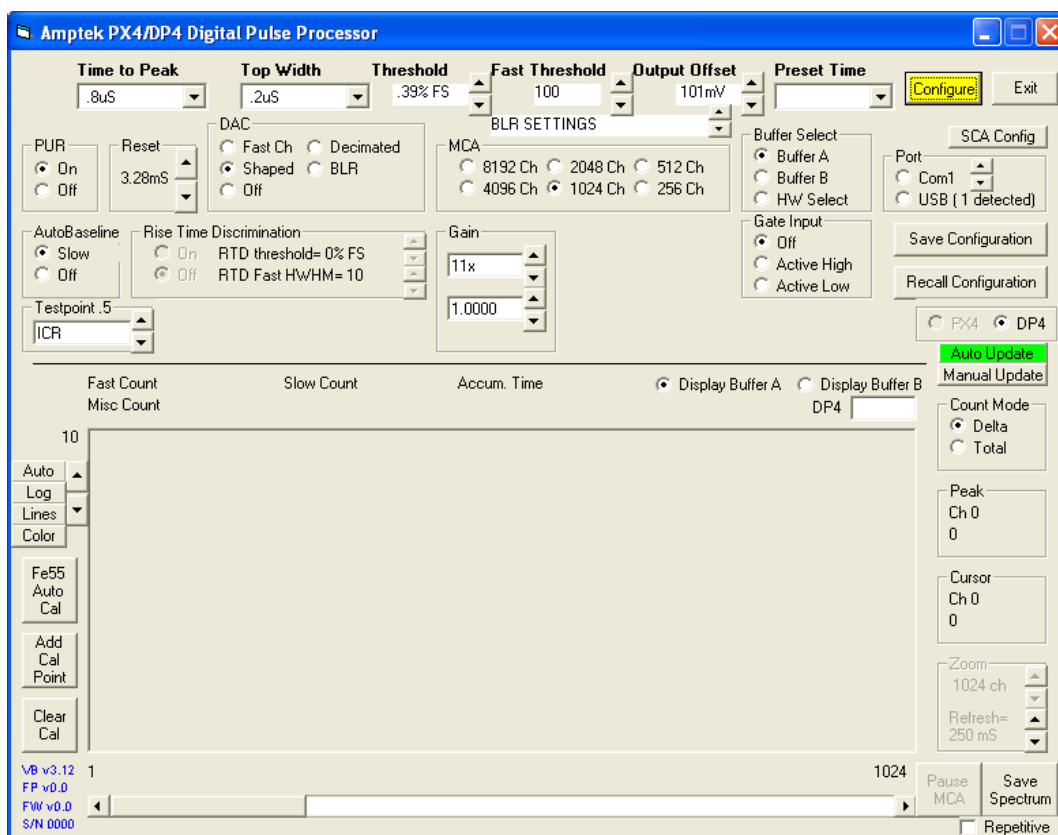
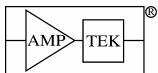


Figure 7. Graphical User Interface for the demonstration data acquisition and control software, which is written in Visual Basic v5.0.

- 3) Turn on power to the DP4. The +3.3V line should draw 100 to 180 mA, while the +/-5 V lines should draw <10 mA. No output should be visible on the screen or on the oscilloscope until the unit has been configured.
- 4) For quick operation, select the proper communications port (COM1, COM2 or USB) on the screen and then click on CONFIGURE, which will turn from yellow to gray. This is not necessarily the optimum configuration but will make the unit operate.
- 5) You can confirm that the DP4 & PC are communicating by checking the lower left-hand corner of the screen. 'FP' (FPGA version), 'FW' (Firmware version) and S/N (Serial Number) will become non-zero when communication is established.





## 3.2 CONFIGURING THE DP4

### 3.2.1 Adjustments via hardware

- 1) Connect an oscilloscope probe to the test point labeled AMP3. The signal should look like the traces shown previously, as the “analog prefilter output” in Figure 4.
- 2) The pulses of interest should have a magnitude of approximately 1V, with an offset of 100 to 200 mV. The offset must be large enough that the signal normally does not drop below ground – it can go below ground during detector reset.

If the polarity is incorrect, refer to section 2.3.1. The coarse gain is adjusted via software, as discussed below. If the signal amplitude is too large, with the coarse gain at its minimum, set the input attenuator as described in section 2.3.1. If the offset is incorrect, adjust R287.

### 3.2.2 Adjustments via software

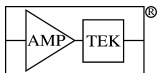
The following parameters can be set via the Visual Basic Software, using the graphical interface shown in

Figure 7 on page 20. Note that the changes are communicated to the DP4 and thereby take effect when the CONFIGURE button is clicked.

- 1) Set the **Time To Peak**, using the pull-down in the upper left hand corner. The peaking time corresponds to about 2.4 times the shaping time of a pseudo-gaussian shaper. Any one of the values between 0.8 and 102.4  $\mu$ sec can be chosen. Once the time to peak has been chosen, the duration of the flat top can be chosen. The range of allowable values is determined by the time to peak.
- 2) Set the **Analog Gain**, using the group of buttons near the middle of the screen. The top box determines coarse gain and allows any of the four values. A gain of 100 will lead to a full-scale energy of approximately 10 keV, using an Amptek XR-100, but this is very approximate and a full calibration should be used. The lower box determines fine gain. The user may use the arrows or may type a new value in the box (configure must be pressed after this).
- 3) Set the **Threshold**. The Threshold setting corresponds roughly to an LLD (low level discriminator) on an MCA. If the peak height of the shaped pulse in the slow channel is below this threshold, it will not be binned in the histogram. The number, e.g. 1.07% FS, corresponds to 1.07% of the full scale in MCA channels. If this threshold is too low, then only low amplitude noise counts will appear on the screen.
- 4) Set the **Fast Threshold**. The Fast Threshold setting applies to the fast signal used for pile-up rejection. Only signals exceeding this threshold can activate the pile-up reject. If this is set too low, then noise activates the pile-up reject, rejecting an excessive number of actual signal counts. If set too high, then piled up events might not be rejected.
- 5) For reset preamps, set Autobaseline to “Slow” and Reset to the longest, 13.1 msec. For continuous feedback preamps, set Autobaseline to “Off”, Reset to “Off”, and set the BLR to some value. Dn 16, Up 16, and Th 256 is often a good starting point.
- 6) **For simplicity, we recommend turning off the various data processing options initially. Set PUR off, RTD off, Gate Input Off. Experience has shown this to be very useful for initial setup and debugging.**
- 7) Set the DAC to “Shaped”. Set the **Output Offset**. This commands a DC offset voltage to the DAC, for display on the oscilloscope. It will have no effect on the spectrum displayed in Visual Basic. If the offset is too low, then the output will sometimes go below zero. The DAC is unipolar and therefore it wraps over, leading to a large voltage. A recommended value is 100 mV.
- 8) After setting these to approximate values, click Configure. The output pulse shape and the spectrum should be close to their desirable values. These parameters can be refined.

## 3.3 TAKING DATA

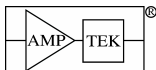
- 1) To accumulate a spectrum for an extended period, select **Count Mode Total**. The counts in the spectrum will integrate over time. By default, the plot autoscales.



- 2) To clear the spectrum, set Count Mode to Delta for an accumulation, then set it back to Total.
- 3) To save data, select the **Save Spectrum** button. The user will be prompted for a file name. The file is written in the standard format of Amptek's PMCA software. This is an ASCII format, with several lines of header information, followed by the spectrum, with one line per channel. It can be read using Amptek's PMCA software or by any software which reads ASCII, e.g. Excel or WordPad.

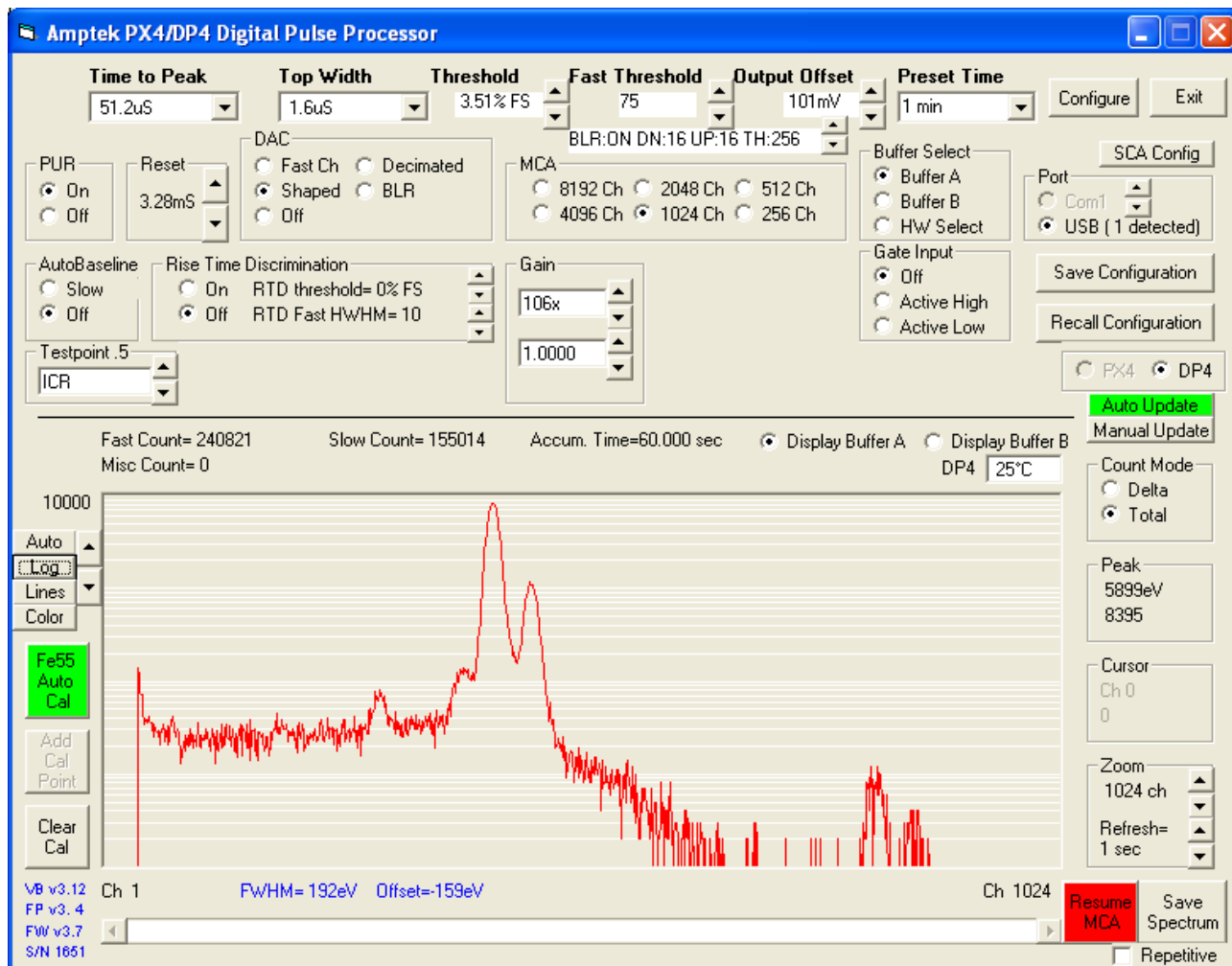
For further information regarding this interface software, please refer to section 4.



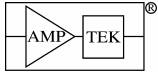


## 4 CONTROL AND DISPLAY DEMONSTRATION SOFTWARE

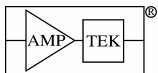
A demonstration user interface program is supplied with the DP4. This software is fully functional, permitting the user to access all of the parameters and features of the DP4. It is intended to demonstrate how to interface with and use the DP4. There are some new controls available for the DP4 Rev. C: The fine gain (set to 1.0000 here), the SCA config button, and an 8k channel selection for the MCA.



- Time to Peak: Sets the peaking time for the shaped pulse.
- Top Width: Sets the width of the trapezoidal flat top for the shaped pulse.
- Threshold: Sets the lower threshold for spectrum accumulation. Works like an LLD on an MCA.
- Fast Threshold: Sets the threshold for the fast channel pile-up reject logic. If this threshold is too low, then valid counts are rejected by noise, leading to a very low throughput.
- Output Offset: The offset voltage of the DAC. Should be high enough to prevent underflow.
- Configure: Sends the configuration parameters from the PC to the DP4. If this is yellow, then configuration parameters have been changed in the PC and not yet sent to the DP4.
- Exit: Exits the program.
- PUR: Enables or disables pile-up reject.
- Reset: Sets the duration of the lockout interval following a reset pulse from the preamplifier.

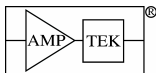


- DAC: Selects which signal is sent to the DAC. If the DAC is off, power consumption is reduced.
- MCA: Selects the number of MCA channels to be used.
- Buffer Select: May use memory buffer A or B, or enable hardware selection of the buffers.
- SCA Config: Clicking on this button will bring up another window, with the SCA controls. In this window, each of the eight SCAs has an enable check box, a lower level, and an upper level. The 'Preset Counts' setting is also found here (it uses the ROI for SCA8.)
- Port: Selects PC serial port COM1-COM8 (for an RS232 interface), or USB Port (for the USB Interface).
- AutoBaseline: Enables AutoBaseline.
- Risetime Discrimination: Turns RTD on, and sets the amplitude and timing thresholds.
- Analog Coarse Gain: Selects one of 4 gain settings. A setting of 100 (10 keV) implies that the full-scale energy will be approximately 10 keV, using an Amptek XR100.
- Digital Fine Gain: Sets the gain to a range of 0.75 to 1.25 in steps of 0.001.
- Gate Input: Enables Gate and selects active High or Low.
- Save/Recall Configuration: Saves or recalls the configuration parameters set in this software. The configuration file is named 'DP4.CFG' and is stored in the current folder.
- Fast Count: Displays the number of counts that have accumulated in the fast channel in the present data acquisition interval.
- Slow Count: Displays the number of counts that have accumulated in the slow channel in the present data acquisition interval.
- Accumulation Time: Displays the duration (real time) of the present data acquisition interval.
- Auto/Manual Update: In Auto update mode, the PC periodically queries the DP4 and downloads the spectrum. In Manual Update mode, the data are only transmitted from the DP4 when the user selects the manual update button. In auto update with the RS232 interface, the update rate is a function of MCA channels: 4 sec for 4096 channels, 2 sec for 2048 channels, 1 sec for 1024 channels, 500 msec for 512 channels, and 250 msec for 256 channels. (8192 channel mode is not supported via the RS232 interface.)
- Count Mode: In Delta mode, the spectrum only displays counts received in the most recent data update interval (i.e., 1 second). The histogram memory is cleared after each update. In Total mode, counts are integrated. Integration begins at the end of the update when Total was pressed and continuous until the update after Delta was pressed. Selecting Delta mode is used to clear the spectrum. (Note: the integration takes place in the DP4, not the host PC.)
- Peak: Indicates the MCA channel with the maximum number of counts, and the number of counts in that channel.
- Cursor: Indicates the MCA channel selected by the cursor and the number of counts in that channel (Left-click with the mouse to set the cursor. The right & left arrow keys move the cursor when the graph is selected.)
- Zoom: Permits the user to zoom in on a subset of the MCA channels. For the RS232 interface, only the selected channels are sent from the DP4 to the host PC, which allows a faster refresh rate. For the USB interface, the DP4 always sends the entire spectrum.
- Save Spectrum: Saves the spectrum to a file. The user will be prompted for a file name. The file is written in the standard format of Amptek's PMCA software. This is an ASCII format, with several lines of header information, followed by the spectrum, with one line per channel. It can be read using Amptek's PMCA software or by any software which reads ASCII, e.g. Excel or WordPad. When saved as a PMCA file the data can be processed by the XRF-FP Quantitative analysis software.



- **Scale:** Sets the vertical scale for spectrum display. By default, the software uses autoscaling based on the maximum counts. The user may also manually scale. Scaling can be either linear or logarithmic.
- **<sup>55</sup>Fe Auto Cal:** Provides a convenient automatic calibration, assuming an <sup>55</sup>Fe source is used. Selects appropriate peaks for the 5.9 and 6.4 keV lines and performs a simple, two-point calibration. (For this to function correctly, the <sup>55</sup>Fe peaks must be the highest peaks in the spectrum.)
- **Add Cal Point:** Permits the user to add additional calibration points for a linear regression.
- **Pause MCA:** Manually starts and stops data acquisition. Only functional with USB.

At the bottom left hand corner of the window is a series of three numbers. These track the configuration of the system at the time this manual was written. VB v3.13 is the version of the Visual Basic display software in use. FP v3.4 is the version of the FPGA in use. FW v3.8 is the version of the embedded software in use.



## 5 PROGRAMMER'S GUIDE

### 5.1 RS232 SERIAL INTERFACE

The DP4 uses the RS232 at 57.6kbaud, with 1 start bit, 8 data bits, 1 stop bit and no parity. No hardware or software handshaking is used. Note that there are no checksums or other checking.

There are two types of data transfers between the DP4 and the host: a configuration packet, and a data request packet. The DP4 will respond to a configuration packet by immediately updating its configuration. It will respond to a data request packet by sending 256 bytes of data.

The configuration packet via RS232 consists of the 64-byte USB configuration packet (described in section 5.2.2), preceded by a sync byte, and followed by an end byte, for a total of 66 bytes.

Byte 1 0xFD (sync)

Bytes 2-65 are identical to the 64-byte USB Configuration packet (see Section 5.2.2)

Byte 66 0xFE (end of config packet)

**NOTE: none of the configuration bytes can have the value 0xFD, 0xFE, 0xFF.**

Data request packet (3 bytes):

Byte 1 0xFD (sync)

Byte 2 requested packet number

Byte 3 0xFF (end of packet request)

[To tell the DP4 to clear the entire MCA buffer, add 0x80 to packet # of the last data request.]  
The DP4 will respond to a data request by sending 256 bytes of data.

MCA Mode	Buffer A Packet Numbers	Buffer B Packet Numbers
256 channels	0x00-0x02 (3 packets)	0x40-0x42
512 channels	0x00-0x05 (6 packets)	0x40-0x45
1024 channels	0x00-0x0B (12 packets)	0x40-0x4B
2048 channels	0x00-0x17 (24 packets)	0x40-0x57
4096 channels	0x00-0x2F (48 packets)	0x40-0x6F
8192 channels	Not supported via RS232	Not supported via RS232
Status packet	0x30	0x70

The spectral packets should be assembled in order into one buffer. The spectral data format is 3 bytes/channel, in order from LSB to MSB, and in channel number from lowest to highest.

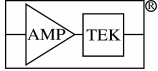
### 5.2 USB INTERFACE

#### 5.2.1 Function Calls

Following are details of the USB function calls in the Visual Basic sample application. Refer to the documentation for the APA USB driver for specifics (on the DP4 CD-ROM), and to the Visual Basic sample application source code to see how each function is used.

**USBDRVD\_GetDevCount** (called by *btnConfigure*, *btnPauseMCA\_Click*, *Timer1\_Timer*, and *Timer2\_Timer*)

This is called prior to opening the USB port, to be sure that a DP4 is available. It's also called prior to most DP4 USB transfers, to be sure that the DP4 hasn't been disconnected or powered off.

**USBDVRD\_OpenDevice** (called by *btnConfigure*)

This opens the device for handle access, which is required for USBDVRD\_VendorOrClassRequestOut.

**USBDVRD\_PipeOpen** (called by *btnConfigure*)

This opens the various DP4 pipes:

USB Pipe	Pipe Function
Pipe 0	Configuration data OUT to DP4 (USB Device Endpoint OUT1)
Pipe 1	Buffer A Status IN from DP4 (USB Device Endpoint IN1)
Pipe 2	Buffer A Spectrum IN from DP4 (USB Device Endpoint IN2)
Pipe 3	Buffer B Status IN from DP4 (USB Device Endpoint IN3)
Pipe 4	Buffer B Spectrum IN from DP4 (USB Device Endpoint IN4)
Pipe 5	Configuration readback IN from DP4 (USB Device Endpoint IN5)

**USBDVRD\_PipeWriteTimeout** (called by *btnConfigure*)

This is used to send the 64-byte configuration packet to the DP4.

**USBDVRD\_CloseDevice** (called by *btnExit\_Click* and *Timer2\_Timer*)

This closes the device handle. Timer2 will close the device if it is open but USBDVRD\_GetDevCount detects no DP4s, due to disconnection or powering down.

**USBDVRD\_PipeClose** (called by *btnExit\_Click* and *Timer2\_Timer*)

This closes the open pipes. Timer2 will close the handles if they are open but USBDVRD\_GetDevCount detects no DP4s, due to disconnection or powering down.

**USBDVRD\_VendorOrClassRequestOut** (called by *btnPauseMCA\_Click* and *Timer1\_Timer*)

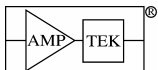
This sends a zero-length 'vendor request' packet to the DP4. (The packet format is described in section 5.2.2.)

The *btnPauseMCA\_Click* routine calls it with a request of 0x82 to disable (i.e pause) the MCA or 0x83 to enable (i.e resume) the MCA.

The *Timer1\_Timer* routine calls it after a spectrum transfer to clear spectrum buffer A (request=0x80) or spectrum buffer B (request=0x81).

There are also commands to turn ON or OFF the four general-purpose pins on JP10.

USB 'Vendor Request'	Function
0x80	Clear spectrum buffer A
0x81	Clear spectrum buffer B
0x82	Disable MCA
0x83	Enable MCA
0x88	Turn OFF JP10 Pin 1 (set to 0V)
0x89	Turn ON JP10 Pin 1 (set to +3.3V)
0x8A	Turn OFF JP10 Pin 2 (set to 0V)



0x8B	Turn ON JP10 Pin 2 (set to +3.3V)
0x8C	Turn OFF JP10 Pin 3 (set to 0V)
0x8D	Turn ON JP10 Pin 3 (set to +3.3V)
0x8E	Turn OFF JP10 Pin 4 (set to 0V)
0x8F	Turn ON JP10 Pin 4 (set to +3.3V)

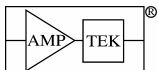
### USBDVRD\_PipeReadTimeout (called by *Timer1\_Timer*)

This is called to retrieve the entire spectrum from either buffer A or buffer B, or the status packet for buffer A or buffer B. The spectral data format is 3 bytes/channel, in order from LSB to MSB, and in channel number from lowest to highest. The status packet format is described in section 5.2.3.

*Note: for proper operation, the calling program should request a byte count of the expected amount plus one. For example, in 1024 channel mode, a spectrum request should ask for 3073 bytes rather than 3072. A status packet request should request 65 bytes, not 64.*

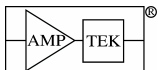
### 5.2.2 USB Configuration Packet Format

Offset	Data bits	Allowed Value	Description
0	D7	0	0=Normal reset lockout, 1=fast reset lockout
	D6-D3	t=0...15	Flat top width=200nS*(t+1)*2 <sup>d</sup>
	D2-D0	d=0...4	Decimation factor=2 <sup>d</sup>
1	D7-D0	0...255	Slow channel threshold
2	D7-D0	0...255	Fast channel threshold
3	D7-D1	-64...+63	Output DAC offset (signed) (-500mV to +492mV)
	D0	0	DAC disabled
		1	DAC enabled
4	D7-D6	0	normal operation
	D5	0	MCA disabled
		1	MCA enabled
	D4-D2	0	MCA 4096 channel mode
		1	MCA 2048 channel mode
		2	MCA 1024 channel mode
		3	MCA 512 channel mode
		4	MCA 256 channel mode
		5	MCA 8192 channel mode
	D1-D0	0	DAC output=fast channel
		1	DAC output=shaped pulse

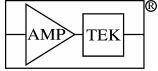


		2	DAC output=decimated input
		3	DAC output= BLR correction
5	D7-D0	1...255	Pileup Reject interval: optimal setting is $(p * 19 + (t + 1) * 4) / 2$
		0	Pileup Reject disabled
6	D7-D4	p=1...8	Peaking Time=800nS*p*2 <sup>d</sup> (See Config byte 0: bits D2-D0, and also Table 1)
	D3-D2	0	Detector reset lockout period=13.11mS (slow) or 819uS (fast) (see Config byte 0: bit D0)
		1	Detector reset lockout period=6.55mS or 410uS
		2	Detector reset lockout period=3.28mS or 205uS
		3	Detector reset lockout period=1.64mS or 102uS
	D1	0	No auto baseline reset during detector reset
		1	Auto baseline reset during detector reset
	D0	0	Disable MCA during detector reset
		1	Do not disable MCA during detector reset
7	D7-D0	0...255	RTD slow threshold
8	D7	1	Normal operation
	D6-D5	0	Analog gain=10.8
		1	Analog gain=20.7
		2	Analog gain=55.4
		3	Analog gain=106.2
	D4	0	RTD off
		1	RTD on
	D3-D0	0...15	RTD time threshold
9	D7	0	50% digital attenuation
		1	Normal operation
	D6	0	0=Baseline Restoration (BLR) off
		1	BLR enabled
	D5-D4	0	BLR Down correction=very slow
		1	BLR Down correction=slow
		2	BLR Down correction=medium
		3	BLR Down correction=fast
	D3-D2	0	BLR Up correction=very slow
		1	BLR Up correction=slow
		2	BLR Up correction=medium
		3	BLR Up correction=fast





	D1-D0	0	BLR correction threshold=very fast
		1	BLR correction threshold=fast
		2	BLR correction threshold=normal
		3	BLR correction threshold=slow
10	D7-D6	0	GATE off
		1	N/A (Gate off)
		2	GATE on, polarity active high
		3	GATE on, polarity active low
	D5-D4	0	Software MCA buffer select, buffer A
		1	Software MCA buffer select, buffer B
		2	Hardware MCA buffer select
		3	N/A
	D3	0	N/A
	D2-D0	0	AUX_OUT=ICR
		1	AUX_OUT=PILEUP
		2	AUX_OUT=HOLD
		3	AUX_OUT=ONESHOT
		4	AUX_OUT=DET_RES (active low)
		5	AUX_OUT=MCA_EN
		6	AUX_OUT=TRIGGER
		7	AUX_OUT=SCA8
11	D7-D0	0-255	Preset time LSB
12	D7-D0	0-255	Preset time Byte2
13	D7-D0	0-255	Preset time MSB [Time=0.1 sec * [MSB*(2 <sup>16</sup> )+Byte2*(2 <sup>8</sup> )+LSB]
14	D7-D0	0	=0
15	D7-D0	0	=0
16	D7-D0	0	=0
17	D7-D0	0	=0
18	D7-D0	0	=0
19	D7-D0	0	=0
20	D7-D0	0	=0
21	D7-D0	0	=0



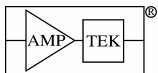
22	D7-D0	0	=0
23	D7-D0	0-255	Fine Gain & Normalizer LSB <sup>1</sup>
24	D7-D0	0-63	Fine Gain & Normalizer MSB <sup>1</sup>
25	D7-D0	0-255	Preset Counts LSB
26	D7-D0	0-255	Preset Counts byte 2
27	D7-D0	0-255	Preset Counts byte 3
28	D7-D0	0-255	Preset Counts MSB [Preset counts=0x0000 if unused]
29	D7-D0	0	=0
30	D7-D0	0	=0
31	D7-D0	0	=0
32	D7-D0	0-255	SCA1 Lower Threshold LSB
33	D7-D0	0-31	SCA1 Lower Threshold MSB
34	D7-D0	0-255	SCA1 Upper Threshold LSB
35	D7	0	SCA1 disabled
		1	SCA1 enabled
	D6-D0	0-31	SCA1 Upper Threshold MSB
36	D7-D0	0-255	SCA2 Lower Threshold LSB
37	D7-D0	0-31	SCA2 Lower Threshold MSB
38	D7-D0	0-255	SCA2 Upper Threshold LSB
39	D7	0	SCA2 disabled
		1	SCA2 enabled
	D6-D0	0-31	SCA2 Upper Threshold MSB
40	D7-D0	0-255	SCA3 Lower Threshold LSB
41	D7-D0	0-31	SCA3 Lower Threshold MSB
42	D7-D0	0-255	SCA3 Upper Threshold LSB
43	D7	0	SCA3 disabled
		1	SCA3 enabled
	D6-D0	0-31	SCA3 Upper Threshold MSB
44	D7-D0	0-255	SCA4 Lower Threshold LSB

<sup>1</sup> 'Fine Gain & Normalizer' setting controls both digital fine gain, and normalizes for different peaking times. The setting is 14 bits in size, and is:

Setting= INT[(FineGain x 8192)/PeakingTime], where

FineGain is in the range 0.75...1.25

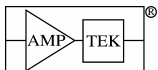
PeakingTime is an integer in the range 1...8 (see configuration byte 6 and Table 1)



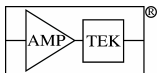
45	D7-D0	0-31	SCA4 Lower Threshold MSB
46	D7-D0	0-255	SCA4 Upper Threshold LSB
47	D7	0	SCA4 disabled
		1	SCA4 enabled
	D6-D0	0-31	SCA4 Upper Threshold MSB
48	D7-D0	0-255	SCA5 Lower Threshold LSB
49	D7-D0	0-31	SCA5 Lower Threshold MSB
50	D7-D0	0-255	SCA5 Upper Threshold LSB
51	D7	0	SCA5 disabled
		1	SCA5 enabled
	D6-D0	0-31	SCA5 Upper Threshold MSB
52	D7-D0	0-255	SCA6 Lower Threshold LSB
53	D7-D0	0-31	SCA6 Lower Threshold MSB
54	D7-D0	0-255	SCA6 Upper Threshold LSB
55	D7	0	SCA6 disabled
		1	SCA6 enabled
	D6-D0	0-31	SCA6 Upper Threshold MSB
56	D7-D0	0-255	SCA7 Lower Threshold LSB
57	D7-D0	0-31	SCA7 Lower Threshold MSB
58	D7-D0	0-255	SCA7 Upper Threshold LSB
59	D7	0	SCA7 disabled
		1	SCA7 enabled
	D6-D0	0-31	SCA7 Upper Threshold MSB
60	D7-D0	0-255	SCA8 Lower Threshold LSB
61	D7-D0	0-31	SCA8 Lower Threshold MSB
62	D7-D0	0-255	SCA8 Upper Threshold LSB
63	D7	0	SCA8 disabled
		1	SCA8 enabled
	D6-D0	0-31	SCA8 Upper Threshold MSB

### 5.2.3 USB Status Packet

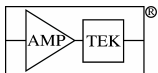
Offset	Data bits	Allowed value	Description
0	D7-D0	0-255	Fast count LSB (Buffer A or B, depending on packet request)



1	D7-D0	0-255	Fast count byte 2 (Buffer A or B, depending on packet request))
2	D7-D0	0-255	Fast count byte 3 (Buffer A or B, depending on packet request))
3	D7-D0	0-255	Fast count MSB (Buffer A or B, depending on packet request))
4	D7-D0	0-255	Slow count LSB (Buffer A or B, depending on packet request))
5	D7-D0	0-255	Slow count byte 2 (Buffer A or B, depending on packet request))
6	D7-D0	0-255	Slow count byte 3 (Buffer A or B, depending on packet request))
7	D7-D0	0-255	Slow count MSB (Buffer A or B, depending on packet request))
8	D7-D4	3-15	FPGA version, major
	D3-D0	0-15	FPGA version, minor
9	D7-D0	0-99	Acc. Time (0-99, 1mS/count)
10	D7-D0	0-255	Acc. Time LSB, 100mS/count
11	D7-D0	0-255	Acc. Time byte 2
12	D7-D0	0-255	Acc. Time MSB
13	D7-D3	3-15	Firmware version, major
	D3-D0	0-15	Firmware version, minor
14	D7-D0	0-255	Serial Number LSB
15	D7-D0	0-255	Serial Number byte 2
16	D7-D0	0-255	Serial Number byte 3
17	D7-D0	0-255	Serial Number MSB
18	D7-D0	0	0 (N/A)
19	D7-D0	0	0 (N/A)
20	D7-D0	0	0 (N/A)
21	D7-D0	0	0 (N/A)
22	D7-D0	-128...+127	Board temp (1 degree/count, signed)
23	D7	0	DP4 detected
	D6	0	N/A
	D5	0	MCA disabled
		1	MCA enabled
	D4-D2	0	N/A
	D1	0	DP4 is unconfigured
		1	DP4 is configured



	D0	0	N/A
24	D7-D0	0-255	General Purpose Counter LSB
25	D7-D0	0-255	G. P. Counter byte 2
26	D7-D0	0-255	G. P. Counter byte 3
27	D7-D0	0-255	G. P. Counter MSB
28-63	D7-D0	0	N/A (Currently unused)



## 6 USE OF THE DP4 WITH AMPTEK'S XR100 DETECTORS

Amptek's DP4 Digital Pulse Processor is easily configured for use with Amptek's family of XR-100 detectors and preamplifiers. The DP4 generally comes configured for use with reset type preamplifiers, which are used in the XR-100CR for Si-PIN. This section is intended to guide a user through the set-up of the DP4 for use with these detectors. Configuration of the DP4 for other preamplifiers is described in section 0.

Some users may already have a PX2 and may be transitioning to the DP4. They can use the PX2 for initial set-up and as a power supply. Section 6.1 describes set-up and configuration for users with a PX2. Other users may not have a PX2 so will set up the DP4 directly. Section 6.2 describes set-up and configuration for users who do not have a PX2. Section X.X describes setup of the DP4 with the PC4-3 power board and the PA-210 peamplifier.

### 6.1 USERS WITH A STANDARD XR100 AND PX2

#### 6.1.1 Set-up

- 1) Set up the PX2 and XR-100 without the DP4. This set-up is described in the PX2 manual, with a block diagram and photograph shown in Figure 8.

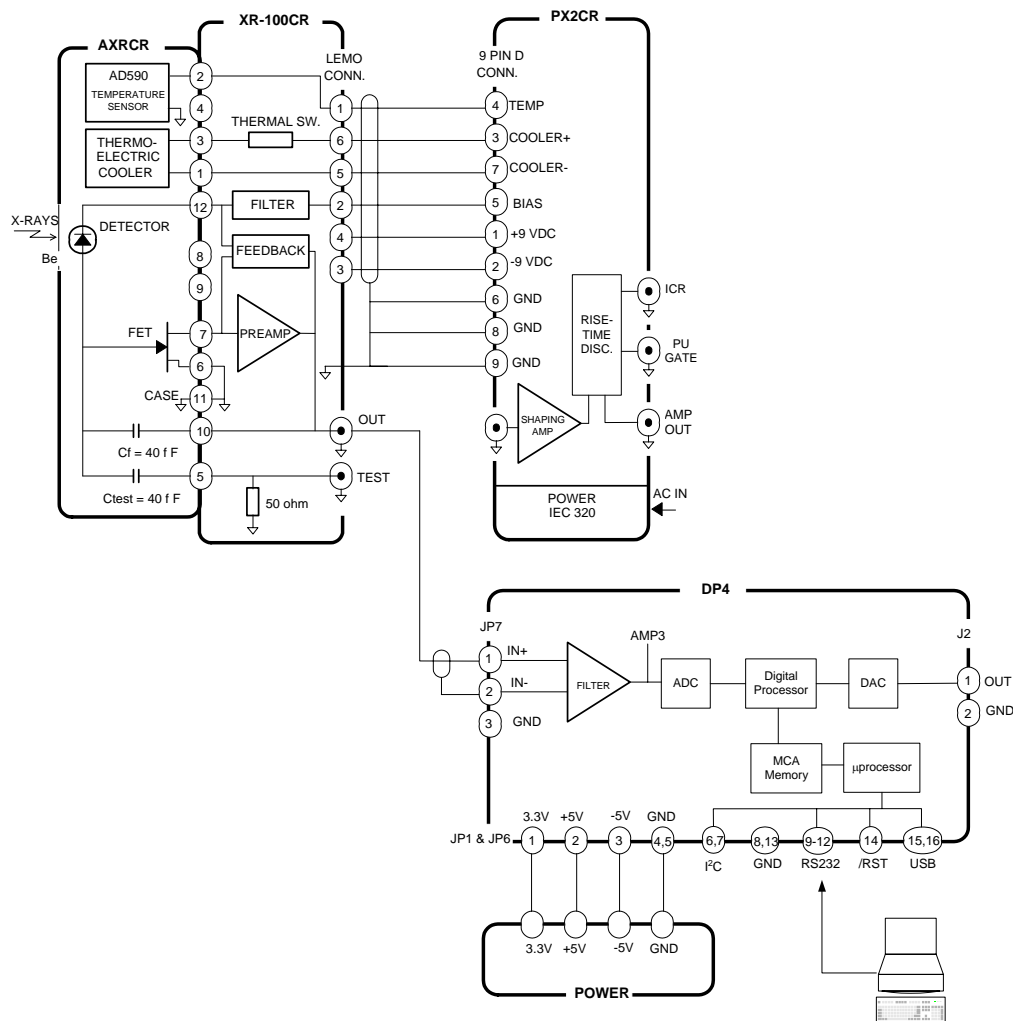
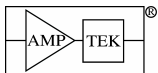


Figure 8. Block diagram of a set-up using both the PX2 and a DP4.



- 2) Connect the XR-100 output to an oscilloscope (using a BNC tee so it is also connected to the PX2 input) and also connect the PX2 output to an oscilloscope. Initially, set the voltage scales to 2 V/div, DC coupled, and the time scale to 100 msec/div or greater.

### 6.1.2 Check Out

- 1) Turn on the PX2. After a few seconds, the oscilloscope should look as shown in Figure 9(a). The XR100 output will have a saw tooth pattern of amplitude about 5V and a period of on the order of a second. This is due to the preamp resets. Place a source in front of the detector and the period of the saw tooth will decrease. Next set the time scale to 10  $\mu$ sec/div. Now the oscilloscope should look as shown in Figure 9(b). This is the shaped pulse from the PX2. If you have an analog MCA, it might be useful to obtain a spectrum. These checks are to verify that the detector, preamplifier, and power supply are functioning properly.

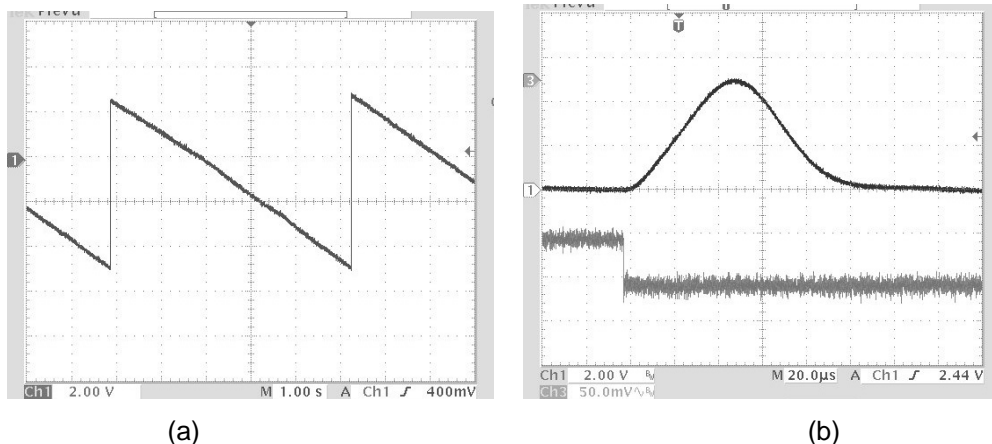
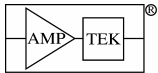


Figure 9. Oscilloscope traces illustrating the normal operation of the XR100 and PX2. (a) This shows the output of the preamplifier, which is input to the PX2 and DP4. The saw tooth shape is due to the reset signals. Note the scales, 2 V/div, 1 sec/div. (b) This shows the preamplifier output (bottom trace) and shaped output of the PX2 (top trace), both due to an X-ray. Note the scales. The preamplifier signal is a few mV step, which is superimposed on the several volt saw tooth shown in (a). The PX2 output is a few volts in amplitude, with a time scale of tens of  $\mu$ sec.

*Note:* When measuring signals with an oscilloscope, it is common for users to first notice the reset (because it is so large) and to confuse this with an X-ray signal. A typical X-ray interaction generates, at the preamp output, a step of a few millivolts (negative), while the reset generates a step of many volts (positive) a few times a second. The shaping amplifier inverts the signal and applies considerable gain, leading to the shaped pulse. The reset pulse is then negative going and saturates. It is important to distinguish between the two.

- 2) Turn the PX2 off. Now connect the DP4 and PX2, as shown in Figure 8. DP4 hardware connections are described in section 2.1. Note that the XR100 output is connected to both the DP4 and PX2, using a BNC tee. The critical connections are:
  - Power: The XR100 is powered from the PX2. The DP4 requires +3.3V and +/-5V.
  - Serial: The RS232 or USB connection from the DP4 to the computer is needed.
  - Signal: The preamplifier output is connected to the DP4 input, JP7. Configure this connector so that the BNC shield is connected to pin 1 while the BNC signal is connected to pin 2. These are differential inputs, so pin 1 is not the DP4 ground. It is vital that a separate ground connection must be made from the XR100 to the DP4. Pin 3 of JP7 can be used. *Note:* Many users have found excessive noise because this ground connection was not made.
  - Output: For debugging purposes, it is convenient to connect an oscilloscope to the DAC output at J2. Pin 2 is ground, pin 1 is signal. This is not necessary for data acquisition but helps initial set-up.





- 3) Start the DP4 software, as described in section 3. Figure 10 below shows a typical screen, illustrating recommended default software configurations for Amptek's XR100 detectors. These may be adjusted by the user but provide reasonable initial values. Turn on the power to the PX2, then to the DP4, then press the "Configure" button on the DP4 software.

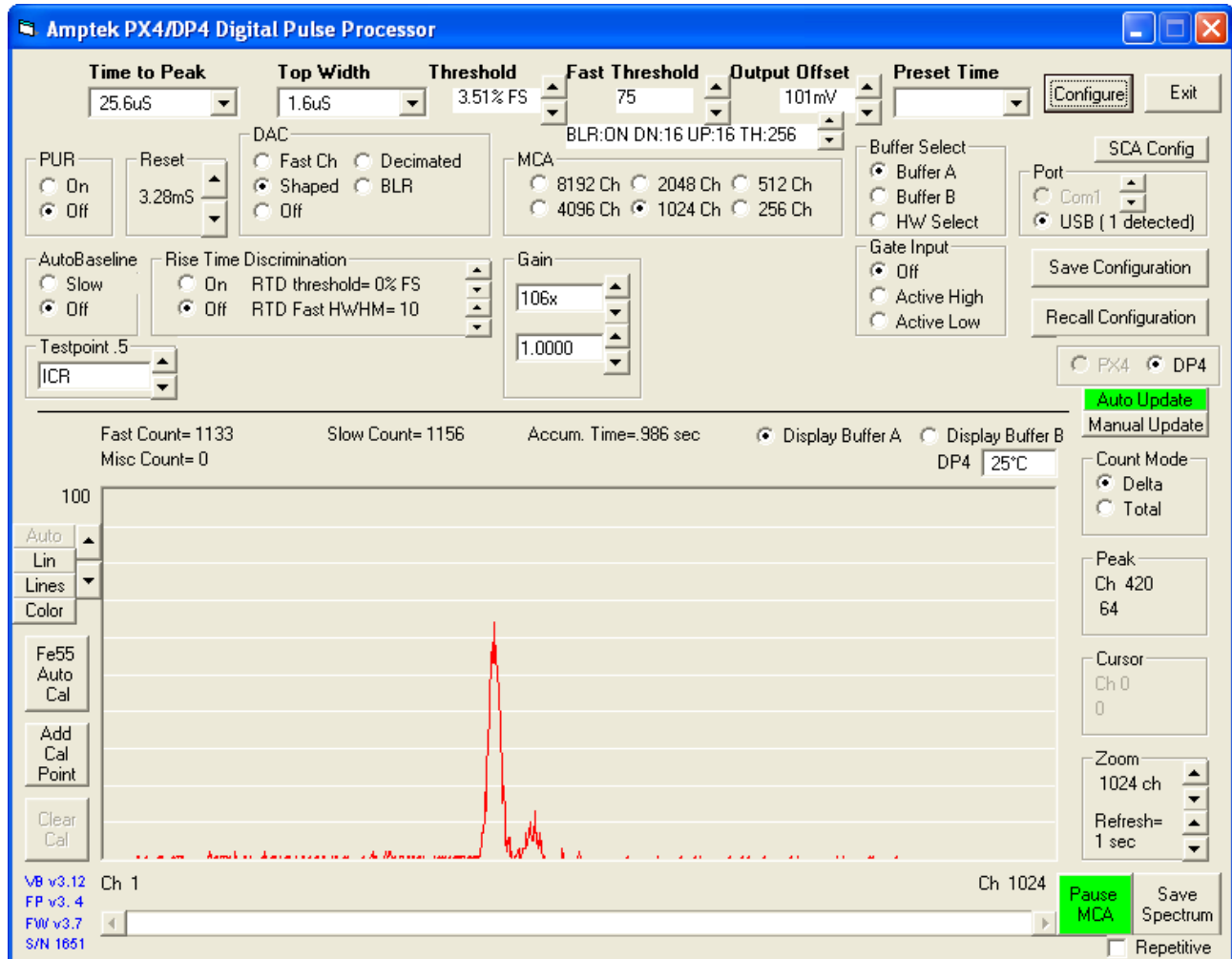


Figure 10. Screen from DP4 demonstration software, showing recommended default values for the software configuration. The peaking time, fast threshold, and slow thresholds are all very important.

- 4) Using an oscilloscope probe, measure the signal at the test point labeled AMP3. It should look like the trace in Figure 11. This is the input to the ADC, prior to the shaping. It is critical that this have (1) a DC offset of about 200 mV, only going negative during resets, (2) a maximum amplitude of about 1 V per pulse, and (3) a fall time of 3.2 usec.

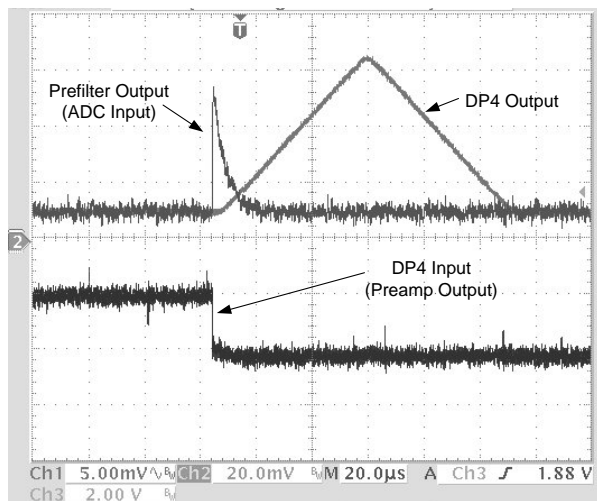


Figure 11. Oscilloscope traces obtained on the DP4, illustrating normal operation. The “prefilter output” is measured at the AMP3 test point.

- 5) Use the oscilloscope to compare the DP4 shaped output (J2) with the PX2 shaped output. The two traces are shown in Figure 11.
- 6) Check the spectrum on the DP4, to see that it matches what is expected for the source and geometry. If the signals at AMP3 and J2 are correct but no spectrum is observed, then check the software configuration.

## 6.2 USERS WITH A STANDARD XR100 WITHOUT A PX2

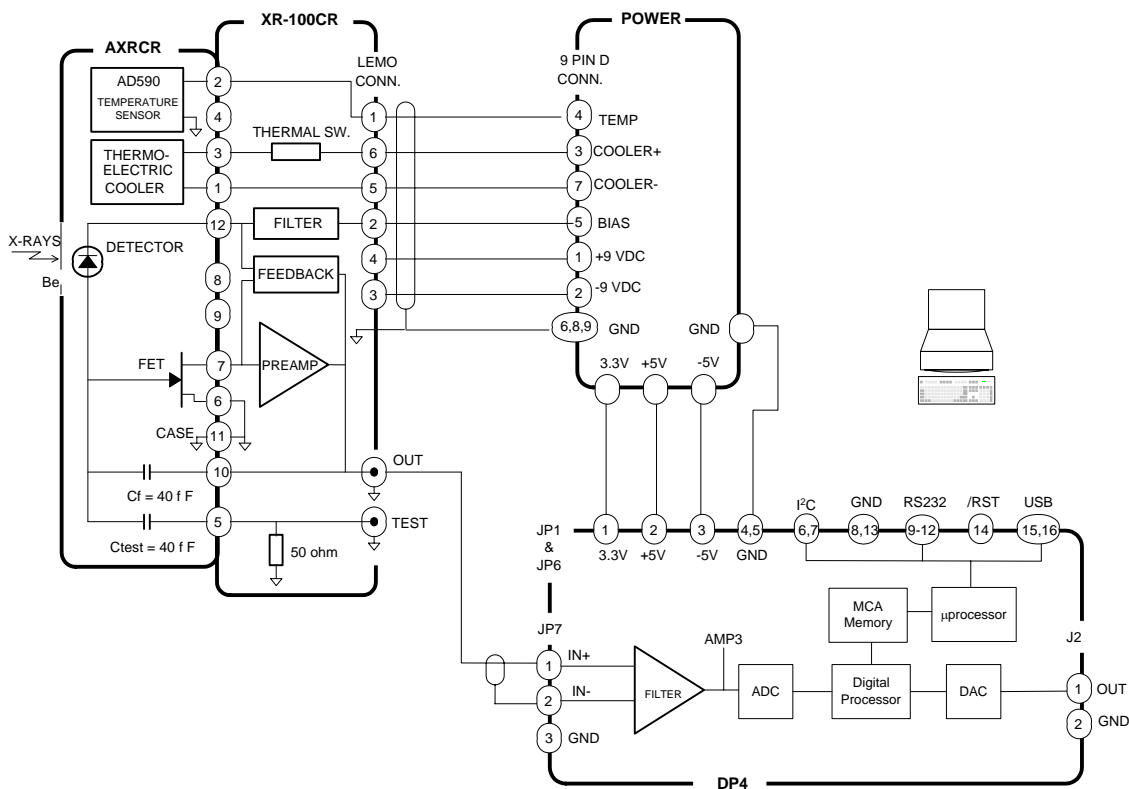
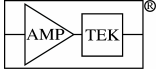


Figure 12. Block diagram of an XR100, DP4, and power supply with no PX2.

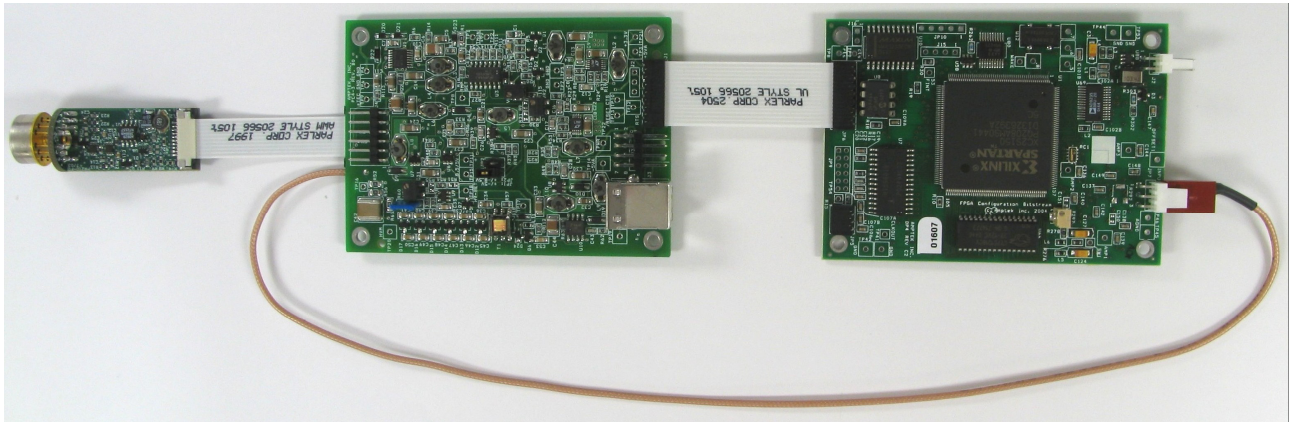
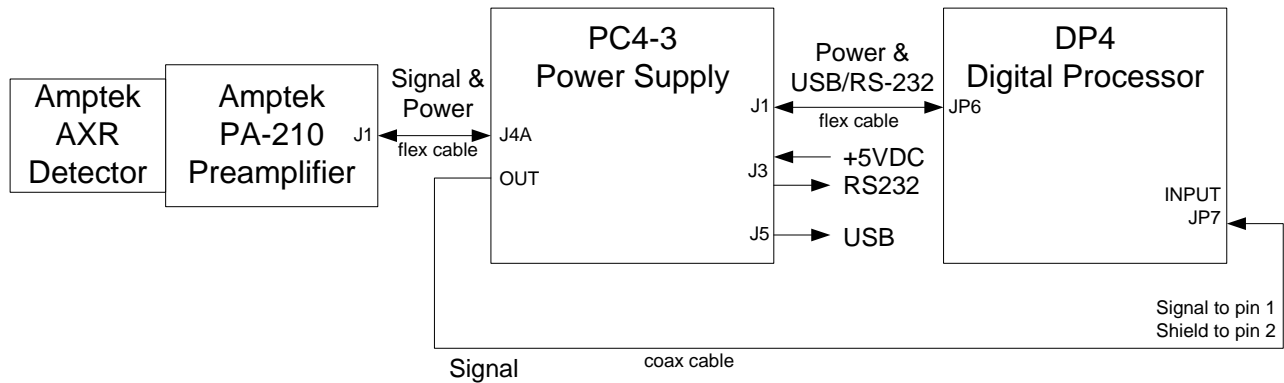


A PX2 is not required, but in its place suitable power supplies must be used. The hardware should be connected as shown in Figure 12. The power supply requirements for the DP4 are given in section 2.2.2. See the XR100/PX2 Manual (section 10 and 11) for specifications on the XR100 power requirements and appropriate setup.

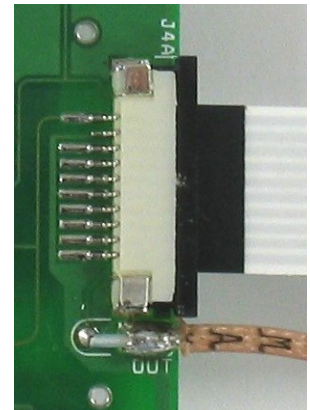
- 1) Make all the connections above and connect the preamplifier output to an oscilloscope. Apply power to the preamp and detector (+/-8V, bias, cooler). Monitor the temperature to verify that the detector is cooling (See XR100CR manual for details).
- 2) The check-out of the system should proceed as described in section 6.1.2 above.

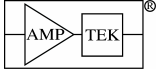
### 6.3 USERS WITH A DP4, PC4-3, AND PA-210 PREAMPLIFIER

Many OEMs use the DP4 together with the PC4-3 power supply board and the PA-210 preamplifier. This total OEM solution is configured as shown below.



The picture to the right is a close up of the J4A connector, which connects between the PC4-3 and the PA-210, and the OUT connection, which connects with a coax cable to the DP4 input (J7: signal pin 1, shield pin 2).





### Use of the DP4 with Tail Pulse Preamps

The DP4 is configured at the factory for particular preamplifier properties, specifically for reset type feedback, for negative input signals of tens of mV, etc. It can readily be used with other preamplifiers, but this requires hardware reconfiguration. This section will guide the user in making these changes.

As shown in Figure 1, the DP4 contains an analog prefilter circuit. The output of this analog prefilter, which is the input to the ADC and can be measured at a test point marked AMP3 on the DP4 board, is shown in Figure 13 as the *Prefilter Output*. The key to adapting the DP4 for various preamps is modifying the prefilter to generate the *Prefilter Output* pulse shape shown in Figure 13. If the signal measured at AMP3 has the proper characteristics, the DP4 will operate properly. This section provides suggestions regarding how the analog prefilter should be adapted for a few common situations, but it cannot cover all possibilities. In any and all cases, measuring the signal at AMP3 will allow the user to determine if the hardware has been properly configured.

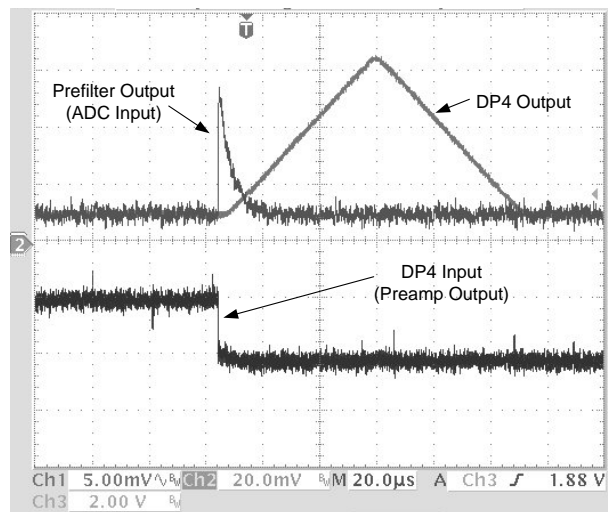
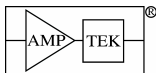


Figure 13. Oscilloscope trace showing the proper signal at AMP3.

The important characteristics of the signal at AMP3, the output of the analog prefilter, are:

- Rise time should be  $>100$  nsec but much faster than the peaking time to be set in the DP4 software
- The decay time must be  $3.2 \mu\text{sec}$  and must be a simple, single pole decay
- The DC offset should be sufficient to keep the ADC input positive. Typically, 200 mV is good. The ADC has a range of 0 to 2V, so if AMP3 drops below 0 V, signal processing anomalies will occur. The DC offset may be increased if necessary. [AMP3 should only drop below 0V during detector reset.]
- The amplitude of the pulse must be about 1V, positive going. The ADC has a range of 0 to 2V, so if AMP3 exceeds 2V, signal processing anomalies will occur.



## 6.4 ANALOG PREFILTER CIRCUIT DESCRIPTION

THIS ENTIRE SECTION MUST BE REDONE FOR NEW REFERENCE DESIGNATORS

The analog prefilter circuit is shown in Figure 14. The main elements are (1) a differential amplifier (U83), (2) a high pass filter with a 3.2  $\mu$ sec time constant, (3) a gain stage (U86), and (4) an amplifier (U82B) providing gain, polarity reversal, and DC offset adjustment. We will now discuss these in more detail.

### 6.4.1 Differential amplifier

This is a (nominally) unity gain differential amplifier, used to reduce common mode ripple. This circuit also permits the user to invert the signal: the output of the differential amplifier should be a negative going pulse, so the preamp signal can be connected to either the inverting or noninverting node of the differential amplifier. This circuit can also provide some gain or attenuation, using the input resistors.

*Note that this signal return is connected to the differential amplifier input and not to DP4 ground. The signal reference does not provide a ground connection. The preamplifier ground must be connected directly to the DP4 ground. Pin 3 of JP7 may be used or some other ground point. Failure to ground the preamp, connecting the preamp ground only to the differential amplifier input, has caused many users significant grounding problems!*

### 6.4.2 High Pass Filter

(R297 + R300) together with C133 form a high pass filter, which provides the 3.2  $\mu$ sec decay seen in the Prefilter Output in Figure 13. Pot R297 is used to fine-tune the time constant. If this pole is set correctly, then the shaped trapezoidal output from the DP4 DAC will have a flat top and a clean tail (no undershoot or overshoot). Setting this pole is very important to the proper operation of the digital pulse processor.

If a preamplifier with a tail is used, i.e. one using resistive feedback, then there will be an undershoot at the output of this filter. This can be seen at AMP2, AMP3, and at the DAC's shaped output. A pole zero resistor must be installed in R292 to cancel the preamp tail. The procedure for doing this is contained in section 6.5.1.

The switch U84 may be used to measure the DC offset which is input to this circuit. This is commonly used with reset-type preamplifiers, which do not need baseline restoration.

### 6.4.3 First Gain Stage

The first gain stage, based on U86, can provide a gain of either 5 or 10. The gain is changed by switch U85A, under command from the microprocessor. Note that any DC output from the high pass filter is amplified by this gain.

### 6.4.4 Final Gain Stage

The final gain stage, U82B, implements several important functions:

- 1) It provides additional coarse gain, of approximately 2 or 10, by switch U85A.
- 2) It inverts the signal. The pulse measured at AMP3 must be positive going.
- 3) It provides a DC offset, by pot R287. The offset input to this amplifier stage ranges from -100 to +100 mV. The pulse measured at AMP3 must have a DC offset sufficient to ensure that the ADC input does not go negative.

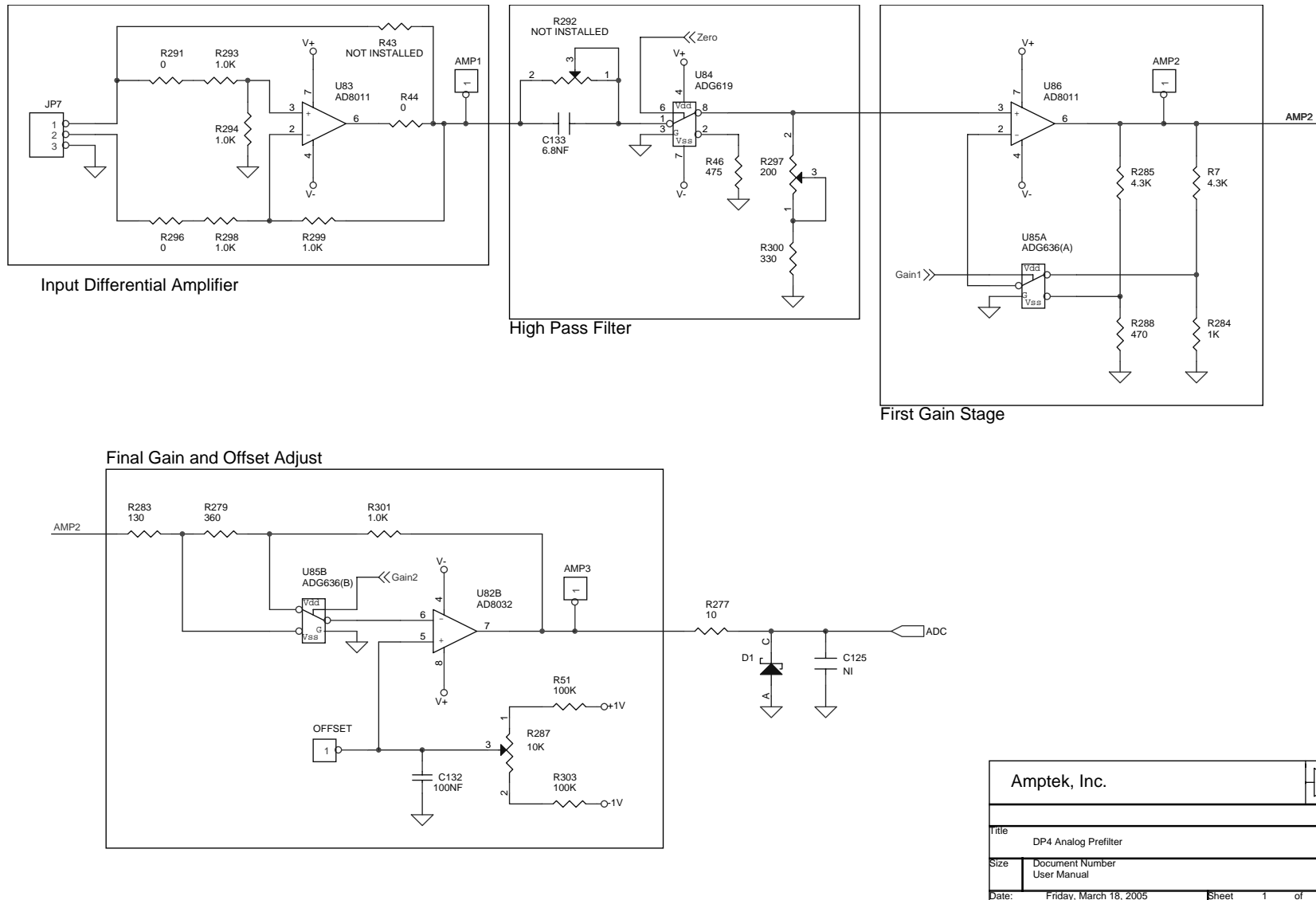
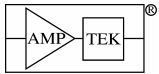
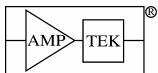


Figure 14. Schematic of the analog prefilter in the DP4. [Renumber]





## 6.5 PROCEDURES FOR COMMON CHANGES

The following sections recommend ways in which the DP4 can be modified to match the output requirements of given preamplifiers.

### 6.5.1 Preamplifier Tail Cancellation

The most common change required is to add a pole zero resistor to cancel the tail of a preamplifier with continuous feedback. The following procedure is suggested:

- 1) Estimate the value of R292. Let  $\tau$  be the preamplifier time constant, the time in which the preamp tail decays to  $1/e$  of its peak value after a step. Then  $R292 = \tau/6.8 \text{ nF}$ . For  $\tau=1 \text{ msec}$ ,  $R292=147\text{k}\Omega$ .
- 2) Install R292. It is usually best to first install a pot to accommodate tolerances in the various components. With the pot installed and set to the approximate value, turn on the system and measure at AMP3 with an oscilloscope, with signals coming through. Look for a long undershoot or overshoot, comparable to the preamp tail. Typical waveforms are shown in Figure 15. If there is an undershoot, decrease R292. If there is an overshoot, increase R292. Once the precise value is found, a fixed resistor may be installed.

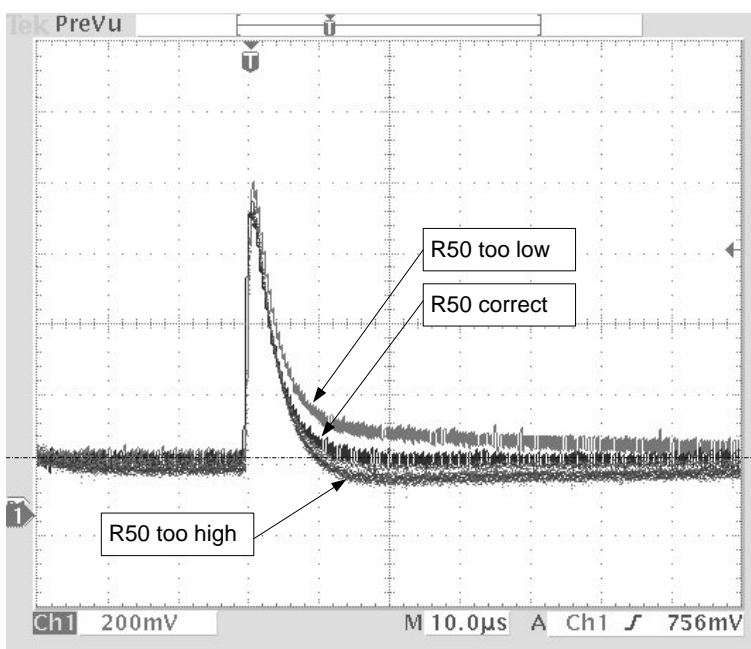


Figure 15. Oscilloscope traces showing AMP3 under several conditions. (a) R292 properly adjusted. (b) R292 too large. (c) R292 too small. When R292 is correct, there is neither undershoot nor overshoot on the tail.

- 3) The presence of R292 will change the time constant of the high pass filter, leading to a slope on the trapezoidal top and to an undershoot or overshoot of short time constant. Typical waveforms are shown in Figure 16. Using the DP4 DAC output, set the peaking time to a short value and the flat top duration as long as permitted. Adjust R297 until the top is flat and no undershoot or overshoot is visible.



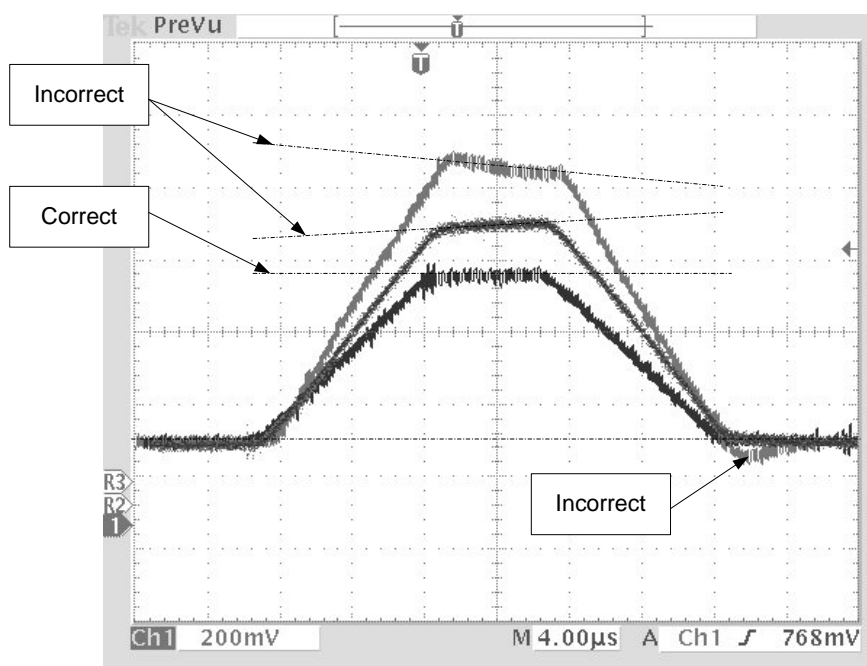


Figure 16. Oscilloscope traces showing the DAC shaped output under several conditions. (a) R297 properly adjusted. (b) R297 improperly adjusted. When R297 is incorrect, the top of the trapezoid is sloped and there is an undershoot or overshoot at the end.

- 4) The presence of R292 also leads to a DC offset into the circuitry. A preamp generally has some DC offset at its output, and R292 combines with (R297+R300) to form a DC divider, coupling a fraction of this offset into the amplifiers, which is then amplified. The DC offset should be measured, first at AMP2 and then at AMP3. If the offset is small enough, then the offset adjust pot R287 can accommodate it. If the offset is a bit larger, then R51 and/or R303 can be decreased to provide more range.
- 5) The diode D1 is only needed to clamp the ADC input in the presence of large, negative reset pulses. We recommend removing it for non-reset preamplifiers.

This procedure will only work if the tail from the preamplifier is a simple exponential (a single pole) and is constant. If there are multiple poles in the preamplifier response, then the dominant pole may be cancelled. The remaining pole(s) may or may not affect proper operation. If the time constant varies, i.e. with temperature or count rate, then the pole will not be cancelled under all conditions.

## 6.5.2 Inversion

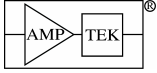
JP7 is the input connector. For positive (negative) going preamp outputs, connect the signal to pin 2 (1). The signal reference from the preamp should be connected to pin 2 (1), respectively.

## 6.5.3 Input Range Adjustment

U83 has a signal range of  $\pm 4V$ . Many preamps have a larger dynamic range, i.e. their output may swing from  $\pm 12V$ . In such cases the input resistors may be used to attenuate the preamplifier signal. Change R291 and R296 (which must be equal) to provide the necessary attenuation. This will cause a slight loss of resolution so should only be used if it is really needed. Alternately, if the preamplifier signal is limited to a smaller range, then this circuit can be configured to provide a small amount of gain, using resistors R293 and R298.

## 6.5.4 Single Ended Operation

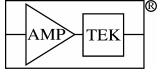
The DP4 is configured at the factor of a differential input, but may be reconfigured for single ended operation. Using differential input has several advantages: it reduces common mode interference (with



proper grounding) and it uses a buffer which separates the output impedance of the preamplifier from the DP4's high pass filter. However, some users prefer single ended operation. To achieve this:

1. Remove resistors R291, R296, and R44.
2. Install a zero ohm resistor in R43.

Pin 1 of JP7, the input, will now go directly to the high pass filter. Pin 2 is not used, while Pin 3 is the ground node.



## 7 DEAD TIME IN THE AMPTEK DP4

Many users have asked “what is the dead time in the DP4”? Often, they are used to working with MCAs which have a “live time clock” which is turned off during “conversion”, the time the peak height is sampled and digitized. But the DP4 has no dead time associated with digitizing the peak amplitude. The incoming pulse stream is digitized at a high rate (20 MHz, every 50 nsec) and then filtered. The peak digital value is determined with no conversion delay (one of the advantages of digital processing). Another advantage of the digital processing arises from the triangular pulse shapes, which are symmetric and return to a true baseline after twice the peaking time. This makes the timing intervals for pile-up and pulse losses very predictable.

In most cases, the reason a user asks for the dead time is to accurately determine the true incoming count rate (ICR). Even though there is no conversion dead time in the DP4, there are counting losses in both the fast and slow channels. This section will explain these losses and how to determine the ICR from the measured rates. This section also explains how to compute the pulse counting losses one can expect.<sup>2</sup>

### 7.1 FAST CHANNEL

The DP4 fast channel signal has a 400 nsec peaking time, and it is this peaking time which is the dead period of the fast channel. It is the rising portion, not the full width. If a second event occurs within 400 nsec of the first, then the second is not counted and a single fast count is recorded. This dead period occurs for 400 nsec after every event, whether recorded or not, so the fast channel counts are described by a paralyzable model. If the true input count rate is  $R_{in}$ , the fast channel dead time is  $\tau_{FAST}=400$  nsec. and the output count rate from the fast channel ( $R_{FAST}$ ) is given by

$$R_{FAST} = R_{in} e^{-(R_{in} \tau_{FAST})} \quad [1]$$

The PX4 does not stop its clock during these dead periods. To estimate the incoming count rate, this equation cannot be used. There is no closed form solution for the true rate, given the fast rate. One can approximate this as a non-paralyzable system and obtain

$$R_{in} \cong R_{approx} = \frac{R_{FAST}}{1 - R_{FAST} \tau_{FAST}} \quad [2]$$

Figure 17 shows  $R_{FAST}$  versus  $R_{in}$  (dark line) and also the throughput, the fraction of counts which are measured by the fast channel (line with filled circles). The accuracy of the approximation in equation [2] is shown by the line with open circles. At  $1 \times 10^5 \text{ sec}^{-1}$ , the fast channel records 96.1% of the incoming counts.  $R_{approx}$ , the approximate correction, has an error of <0.08% at this rate. For most purposes, the fast channel count rate measurement is the best way to estimate the true incoming count rate.

<sup>2</sup> This discussion and the equations are based on the discussion by G.F. Knoll, *General properties of radiation detectors*, Chap 4 in **Radiation Detection and Measurement**, John Wiley & Sons, New York (1989), pp 120-122

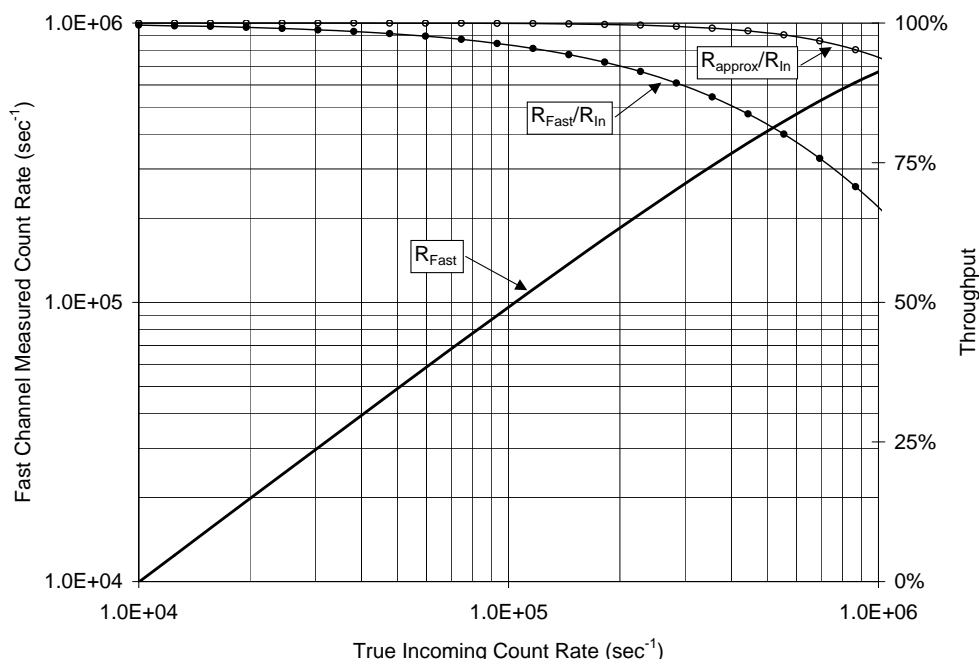


Figure 17. Plot showing the throughput of the fast channel versus input count rate.

## 7.2 SLOW CHANNEL

The slow channel count rate varies depending on the pile-up rejection settings. Figure 18 shows two cases. In the plot on the left, the two pulses are separated in time by more than the peaking time. They can clearly be recognized as separate pulses and accurate peak heights can be measured. Both are valid events and will be recorded in the spectrum and in the slow channel counts. Because of the symmetry of the triangular shaping, if the pulses are separated by more than the peaking time, they are not piled up. This is unlike an analog shaper, where the pulses are asymmetric.

In the plot on the right, the two pulses are separated by less than the peaking time. Only a single pulse occurs at the shaped output, with amplitude near the sum of the two. If pile-up rejection is turned off, then this is recorded as a single event with incorrect amplitude. If pile-up rejection is turned on, then both events are rejected. Nothing appears in either the slow channel counts or in the spectrum.

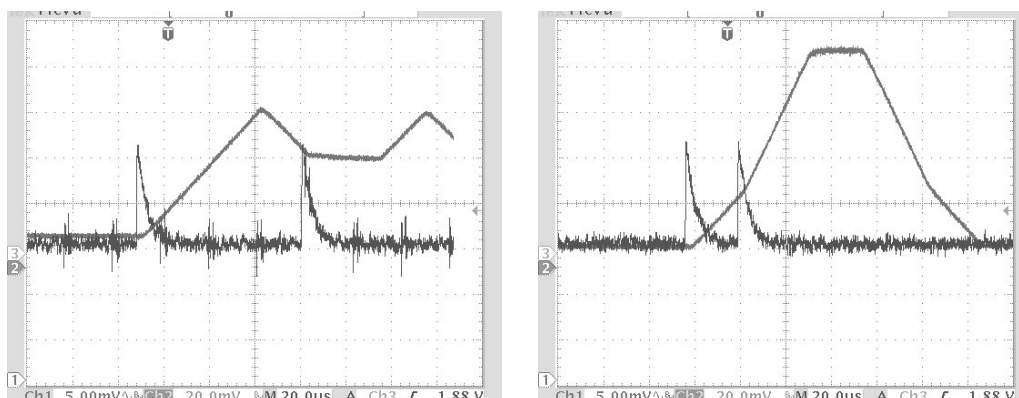
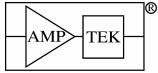


Figure 18. Oscilloscope traces showing (left) two pulses which are separately detected and accurate pulse heights measured and (right) two pulses which overlap in time. These plots show the output of the analog prefilter (the tail pulses) and the shaped output.

The window for pile-up rejection is  $(1 + 3/16)$  of the peaking time. If pile-up reject is on, this is the dead period and the equation for OCR reflects the fact that two events are removed. If pile-up reject is off, the



dead period is closer to the peaking time (plus some small jitter) and only one event is removed. The measured rates are

$$R_{PUR\_Off} = R_{In} e^{(-R_{In} \tau_{peak})}$$

$$R_{PUR\_On} = R_{In} e^{(-2R_{In}(19/16)\tau_{peak})} \quad [3]$$

Figure 19 shows computed (lines) and measured (circles) output count rates versus input count rates, at several peaking times. The computations use the formula in equation [3]. Excellent agreement is clearly seen between measurement and calculations.

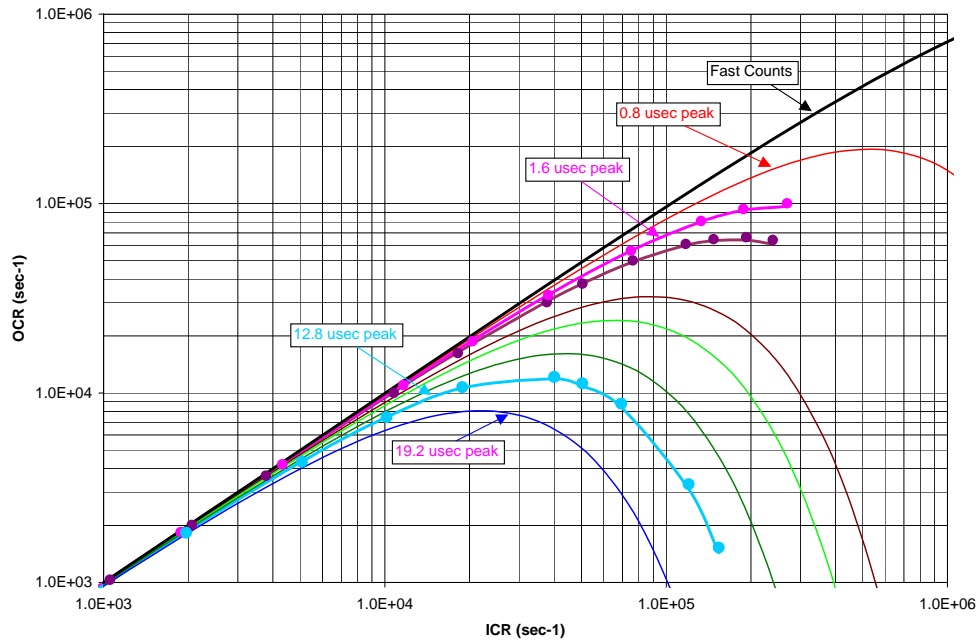
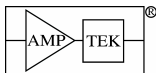


Figure 19. Plot showing measured and computed input and output count rates, with pile-up rejection on, for various peaking times.

### 7.3 ACQUISITION TIME

The DP4 provides the fast counts, the slow counts, and the “acquisition time”. It is important to define this acquisition time. This is the real elapsed time during which data are being acquired. The real time clock is turned off during certain events, including data transfers over the serial bus and also including reset intervals. If a reset preamplifier is used, and the DP4 is configured for a certain reset time period, then acquisition is shut down during the reset period and the acquisition clock is stopped. This acquisition time is measured using a typical 20 ppm crystal oscillator so is quite accurate. The true count rate should be computed using the actual acquisition time rather than the nominal data transfer time.

Data transfers occur based on an approximate real time clock. For example, one might configure the DP4 to update every second. When the data transfer occurs, the acquisition time is shown and this will probably differ from the nominal “1 second”, due to the approximate clock and also due to reset losses. A typical value is 1.05 second. At high count rates, a reset preamp resets more often, and so there is less acquisition time per transfer. In this case, the acquisition time might become 0.85 seconds. On the screen, this time is displayed along with the fast counts and the slow counts during the same interval. The actual count rate is found by dividing the observed counts by the observed acquisition time, 0.85 seconds for this example.



## 7.4 TIMING SUMMARY

In the following, the pulse separation time is denoted  $T$ .

- 1)  $T > (19/16)\tau_{\text{peak}}$  : Both are recorded in the spectrum with correct amplitude, and both are recorded in both fast and slow counts. True for PUR on and off.
- 2)  $(19/16)\tau_{\text{peak}} > T > 400 \text{ nsec}$ : With PUR on, neither is recorded in the spectrum or in slow counts but both are recorded as fast counts.
- 3)  $\tau_{\text{peak}} > T > 400 \text{ nsec}$ : With PUR off, a single event is recorded in the spectrum (with incorrect amplitude), a single slow count is recorded, but both are recorded as fast counts.
- 4)  $400 \text{ nsec} > T$ : A single event is recorded in the spectrum (with incorrect amplitude), a single slow count is recorded, and a single fast count is recorded. True for PUR on and off.

This presumes that both events are above both the fast and the slow thresholds. For signal amplitudes near threshold, one or both might not be recorded. The fast and slow thresholds are different (the fast threshold is usually higher than the slow) so an event may be recorded in one channel but not the other.

## 8 TROUBLE-SHOOTING GUIDE

### Configuration

- If the fast threshold is too low, then noise counts will trigger the pile-up reject circuit. This can veto most or all of the actual events. This threshold can be raised or the PUR can be disabled.
- If the fast threshold is too high, then piled up events might not be rejected.
- Both pile-up rejection (PUR) and risetime discrimination (RTD) are used to select those pulses which are recorded. If the settings are wrong, the incorrect pulses are recorded and in many cases, no pulses are recorded. If no spectrum appears, the first diagnostic step should be to turn off PUR and RTD

### Grounding

- Care must be taken in grounding the DP4. In particular, noise problems may occur if the signal ground that connects the preamplifier to the DP4 input is a power return.
- Amptek has observed at least one Dell laptop that injects significant current via the RS232 ground into the DP4, which seriously upsets performance. Our solution is to use a 3-prong to 2-prong AC adapter on the laptop, which disconnects the laptop power supply from AC ground.

## 9 INDEX

analog prefilter .....	3, 6, 15, 39, 40, 41	pulse shaping.....	3, 5, 15, 21
auto baseline .....	7, 16, 21, 24, 29	reset preamplifier ...	4, 6, 12, 16, 21, 23, 28, 34, 39
baseline restoration .....	7, 16, 29	risetime discrimination .....	8, 17, 21, 24, 29
gate .....	9, 17, 24, 29	RS232 interface .....	19, 24
MCA.....	4, 17, 23, 24	serial interface.....	4, 10, 11, 13, 19
pile up rejection.....	7, 17, 21, 23, 28	threshold .....	7, 8, 17, 21, 23, 28, 48
preamplifier .....	3, 4, 6, 11, 12, 16, 20, 34, 39, 42	USB interface.....	19, 24

Current version as of manual release date: PCB rev C2, VB rev 3.13, FP rev 3.4, FW rev 3.8

**END OF DOCUMENT**